

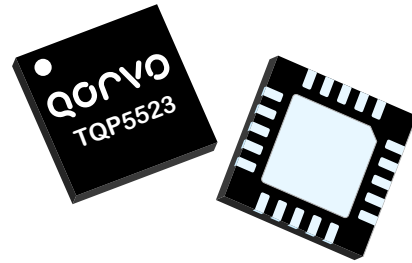
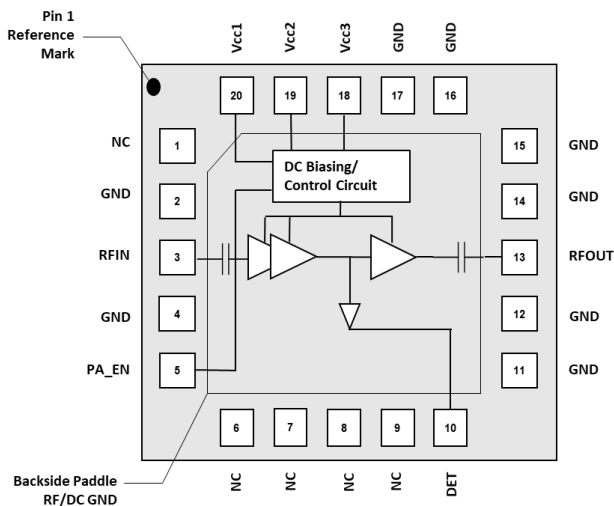
Product Overview

The TQP5523 is high power WLAN power amplifier module that contains internally matched 3-stage PA, compensated DC biasing circuit and output power detector. This PA module provides high gain (32 dB), high linearity, industry leading EVM floor, and excellent spectral purity for wideband OFDM applications. The architecture and interface are optimized for most stringent EVM requirements of next generation 802.11.ac WLAN devices.

The TQP5523 features chipset logic compatible control voltages that draw very low current to facilitate ease of use and compatibility with current and future transceiver generation. With its optimized power dissipation, the amplifier module is well suited for implementation into next generation MIMO configurations and well designed to work with or without digital pre-distortion (DPD).

The TQP5523 is manufactured using Qorvo's high-reliability HBT technology and is assembled in a small footprint 4.0 mm x 4.0 mm x 0.85 mm 20 pad QFN package.

Functional Block Diagram



20 Pad 4.0 x 4.0 x 0.85 mm QFN Package

Key Features

- Fully Integrated, 802.11ac Power Amplifier Module With Power Detector
- Internally Matched Input/Output
- Temperature Compensated Bias Network
- High Gain = 32 dB
- Integrated CMOS Compatible Logic and Shutdown
- $P_{OUT}=+23.5$ dBm (typ.) at -30 dB EVM (802.11n/HT40/MCS7)
- $P_{OUT}=+16$ dBm (typ.) at -40 dB EVM (802.11ac/VHT80/MCS9)
- $P_{OUT}=+21$ dBm (typ.) at -37 dB EVM (802.11ac/VHT80/MCS9)
- Supply Voltage: +3.3 V to +5.0 V
- Leadless 4.0 x 4.0 x 0.85 mm SMT Pb-Free Package

Applications

- 802.11a/n/ac Wireless LAN Systems
- CPE (Set Top Box, Routers, Gateways)
- WiFi Access Points and Small Cells
- Telematics
- Gaming and Infotainment
- Portable Devices
- Point-to-point and Backhaul
- ISM Band

Ordering Information

Part No.	Description
TQP5523	2500 Pieces on a 13" reel (standard)
TQP5523-EVB	Assembled Evaluation Board

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	-40 to 150 °C
Case Temperature, Survival	-40 to 100 °C
RF Input Power, CW, 50 Ω, T = 25 °C	+5 dBm
Device Voltage	+6.0 V

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
V _{CC1} , V _{CC2} , V _{CC3}	+3.3	+5.0	+5.25	V
T _{AMB}	-30	+25	+85	°C
T _j (for >10 ⁶ hours MTTF)			+170	°C

Electrical performance is measured under conditions noted in the electrical specifications table. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications – DC Characteristics

Parameter	Conditions ⁽¹⁾	Min	Typ	Max	Units
Quiescent Current	No RF		195	250	mA
Operational Current	P _{out} = +21 dBm, 802.11ac/MCS9/HT80		300		mA
TX Shut Down Current	PA_EN= Low, No RF		8		μA
PA Enable Voltage	Input Voltage for High State	+1.8	+3.0	V _{CC1}	V
	Input Voltage for Low State		0	+0.45	V
PA Enable Current			10	100	μA
Rise/Fall Time			0.4	0.8	uS
Thermal Resistance, θ _{jc}	Junction to backside paddle		35		°C/W

Notes:

1. Test conditions unless otherwise noted: V_{CC1}, V_{CC2}, V_{CC3} = +5.0 V, Temp = +25°C.

Logic Truth Table

PA Mode	PA_EN State
Disabled	Low
Enabled	High

Electrical Specifications

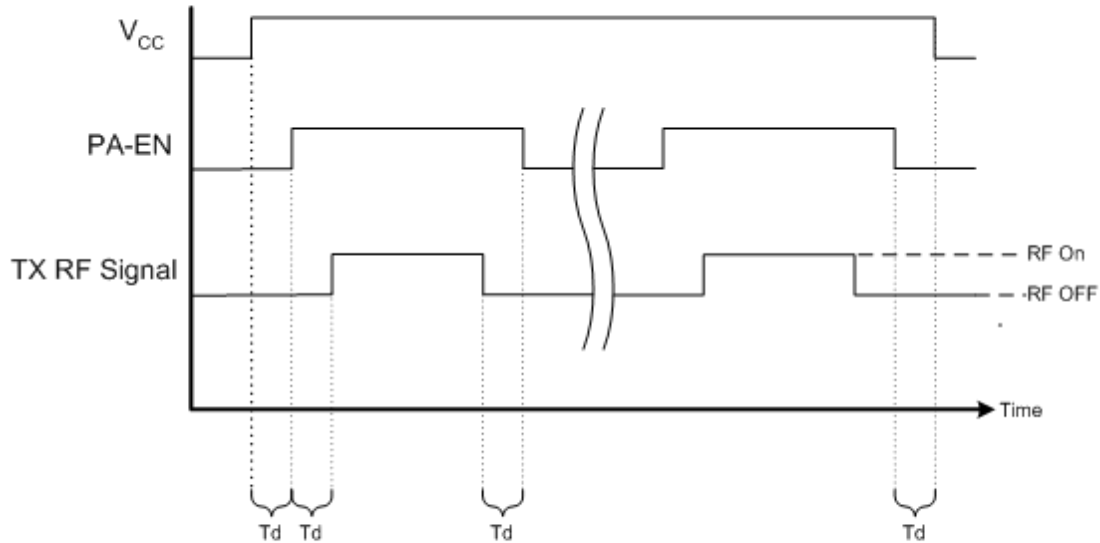
Parameter	Conditions ⁽¹⁾	Min	Typ	Max	Units
Operational Freq. Range		4900		5925	MHz
3dB Bandwidth	At each 802.11ac VHT80 channel	4850		6430	MHz
Saturation Power (Psat)	f =4900 – 5250 MHz		26.5		dBm
	f =5250 – 5925 MHz		31		
Small Signal Gain	f =4900 – 5250 MHz	26	28	34	dB
	f =5250 – 5925 MHz	29	32	37	
Gain Out of Band	Absolute gain, f =3433 – 3917 MHz		0		dB
	Absolute gain, f=1716 – 1959 MHz		-50		
Gain Flatness Across Band	For any 80 MHz BW, 802.11ac / VHT80		+/- 0.3		dB
Spectral Emission Mask Margin Relative to 11ac standard (802.11ac/HT20/MCS0)	Pout = +24 dBm, f =5150 – 5250 MHz		5		dB
	Pout = +24 dBm, f =5250 – 5725 MHz		5		
	Pout = +24 dBm, f =5725 – 5925 MHz		5		
PA Noise Figure			7		dB
Input Return Loss			8		dB
Output Return Loss			10		dB
CW Signal Phase Variation Harmonics (2f ₀)	Pout = +15 dBm to +21 dBm		1.0		deg
TX Harmonics (2f ₀) (802.11ac/VHT80/MCS9)	Pout = +20 dBm, f =5150 – 5250 MHz		-45		dBm/MHz
	Pout = +24 dBm, f =5250 – 5725 MHz		-45		
	Pout = +24 dBm, f =5725 – 5925 MHz		-45		
TX Harmonics (3f ₀) (802.11ac/VHT80/MCS9)	Pout = +24 dBm, f =5150 – 5250 MHz		-45		dBm/MHz
	Pout = +24 dBm, f =5250 – 5725 MHz		-45		
	Pout = +24 dBm, f =5725 – 5925 MHz		-45		
DEVM (802.11n/HT40/MCS7)	Pout = +23.5 dBm		-30		dB
DEVM (802.11ac/VHT80/MCS9)	Pout = +16 dBm		-40	-35	dB
	Pout = +21 dBm		-37	-32	
DEVM (802.11ac/VHT20/MCS0)	Pout = +24.5 dBm		-28	-25	dB
Detector Voltage	No RF		+0.35		V
	Pout = +24.5 dBm	+0.7	+0.9	+1.0	
Stability	Pout = +24.5 dBm, VSWR = 6:1, all phases	All non-harmonically related outputs < -50 dBc/100 kHz			-
Ruggedness	Pout = +24.5 dBm, VSWR = 6:1, all phases	No Damage			-

Notes:

1. Test conditions unless otherwise noted: 25°C, Vcc1, Vcc2, Vcc3 = 5.0V, PA Enable High = 3.0V, TQ EVB , -45dBm EVM source

Timing Diagram

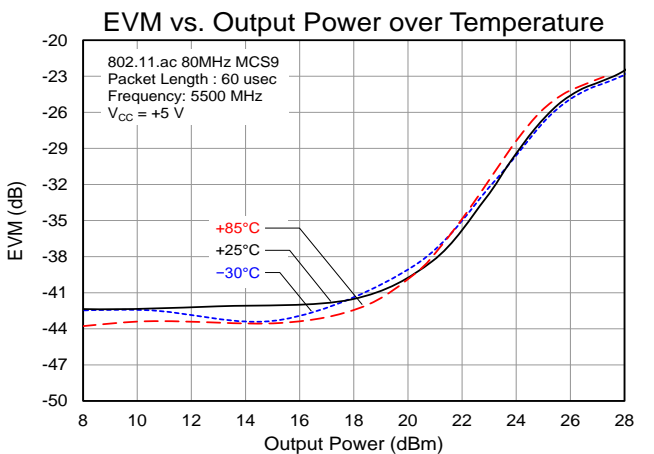
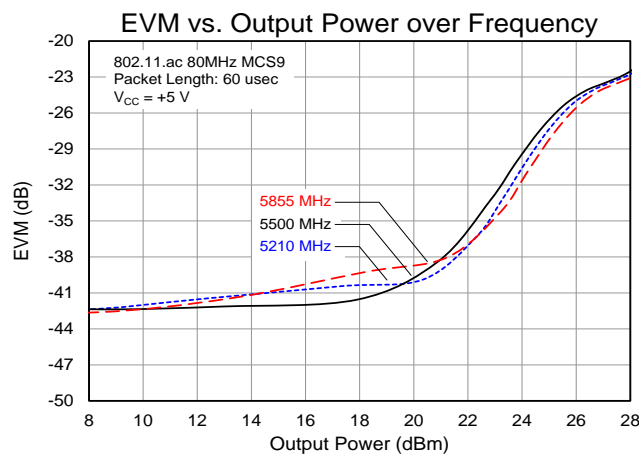
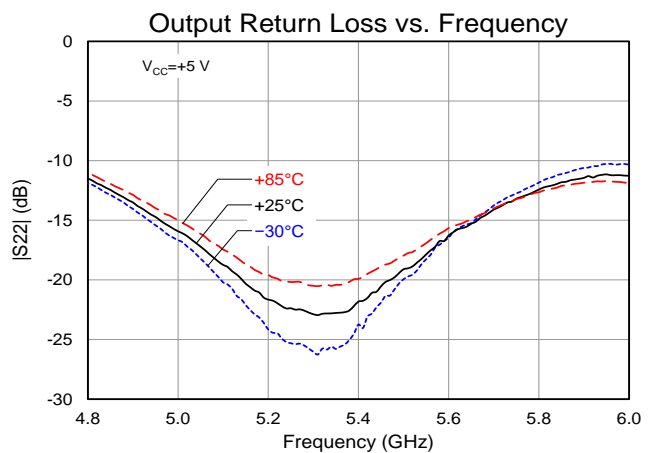
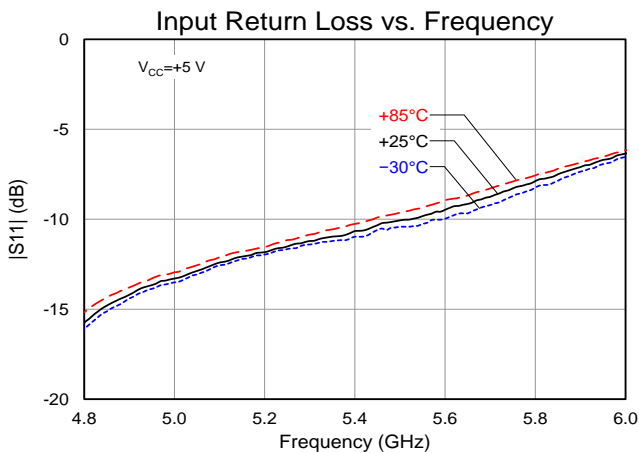
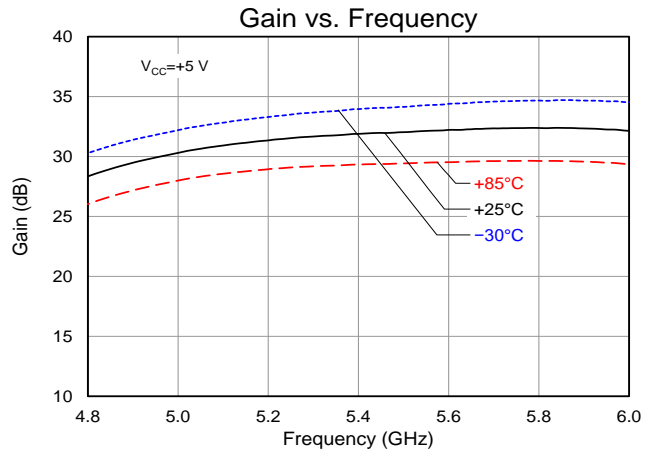
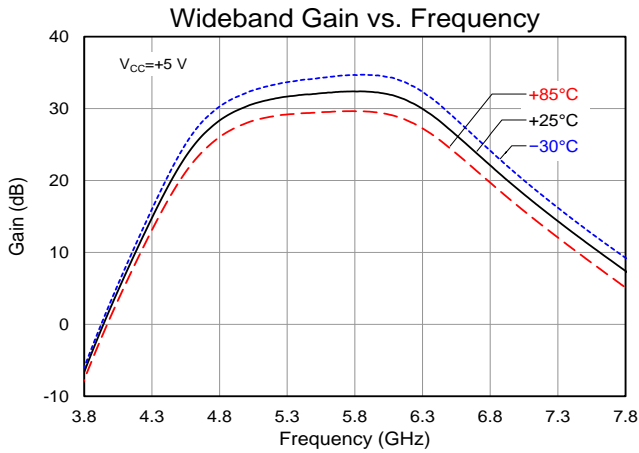
Transmit Timing Diagram
RF/DC Power On/Off Sequence



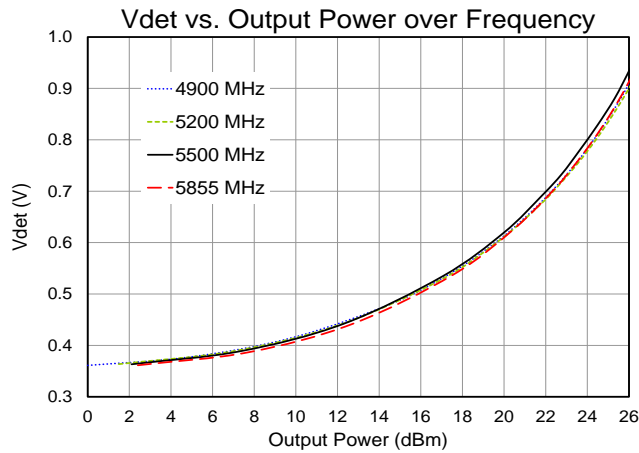
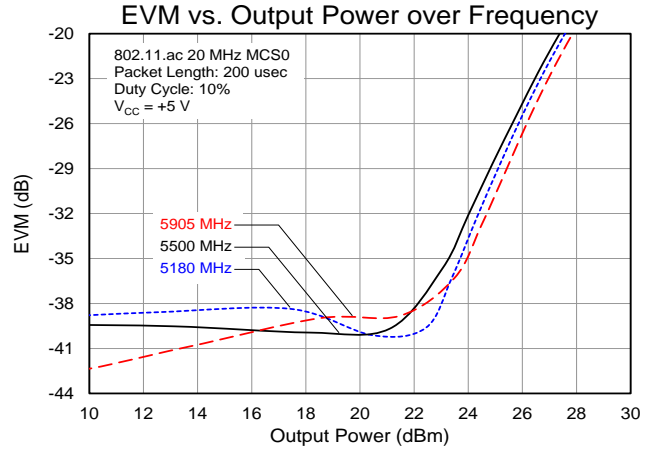
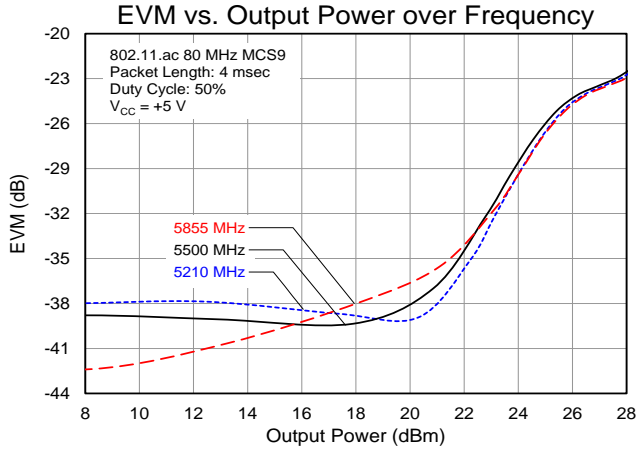
Notes: DC and RF signal levels per data sheet specification.
Observe the timing sequence shown in the diagram above and described below.

- Apply V_{CC} prior to turning on or pulsing PA enable.
- Turn off PA enable prior to turning off V_{CC} .
- Turn on PA enable prior to applying RF signal.
- Turn off RF signal prior to turning off PA enable.

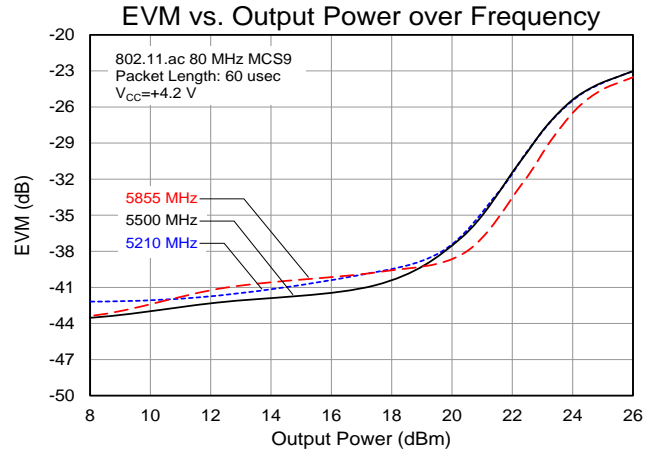
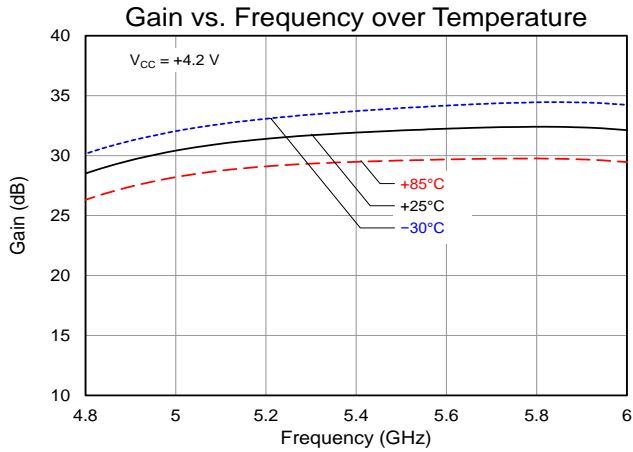
Performance Plots $V_{CC} = +5 V$



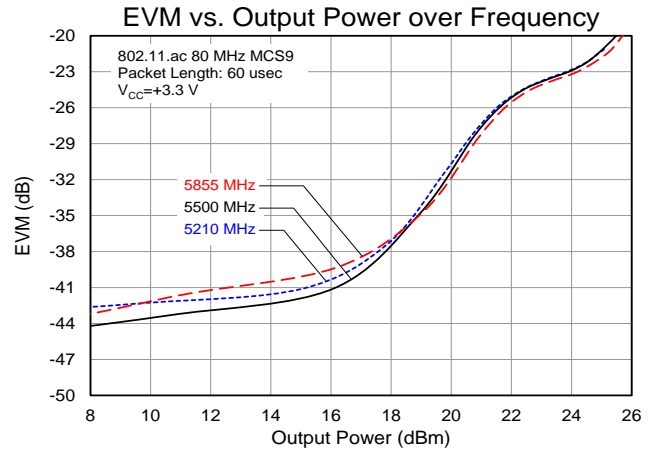
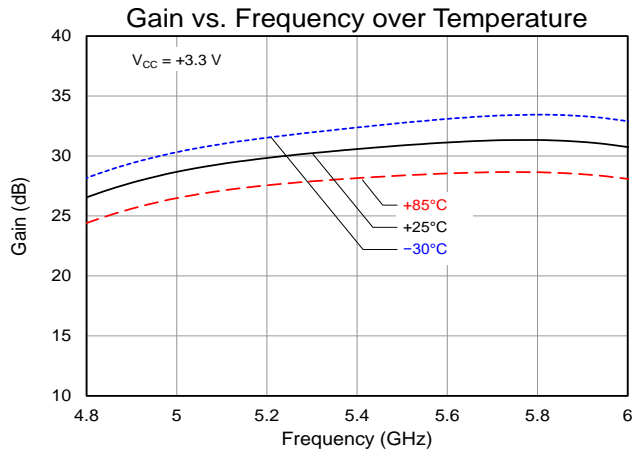
Performance Plots $V_{CC} = +5\text{ V}$ (cont.)



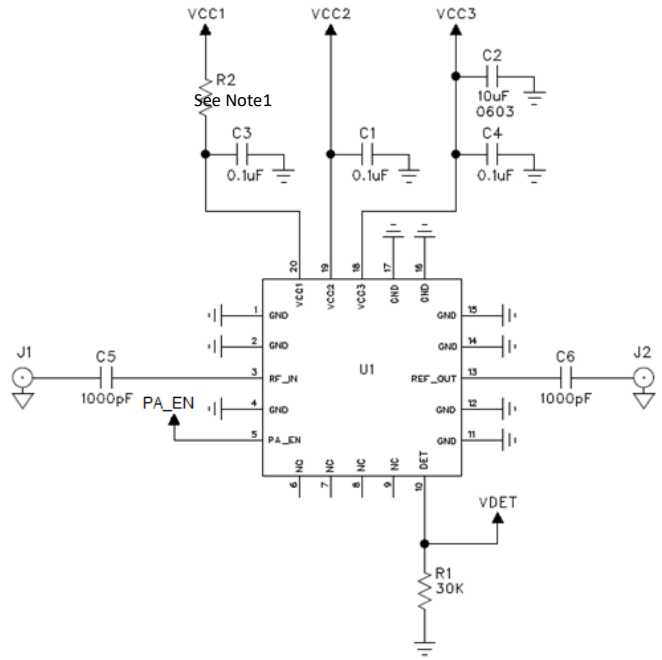
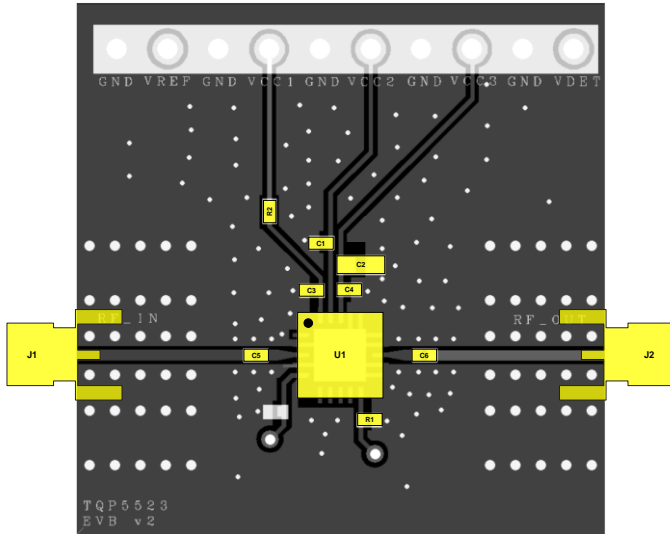
Performance Plots $V_{CC} = +4.2\text{ V}$



Performance Plots $V_{CC} = +3.3\text{ V}$



Evaluation Board - TQP5523-EVB



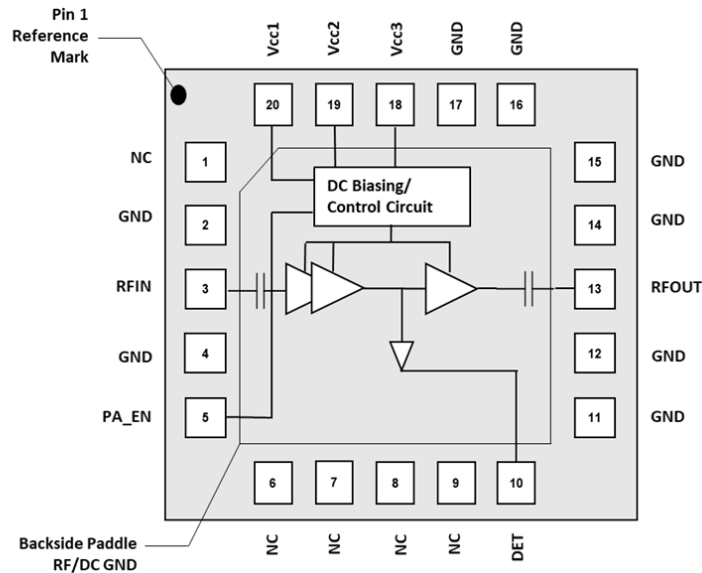
Bill of Material

Ref Des	Value	Description	Manuf.	Part Number
n/a	n/a	Printed Circuit Board		
U1	n/a	High Power WLAN 5GHz PA	TriQuint	TQP5523
C5, C6	1000 pF	Capacitor, Chip, 0402, 5%	various	
C1, C3, C4	0.1 uF	Capacitor, Chip, 0402, 10%	various	
C2	10 uF	Capacitor, Chip, 0402, 10%	various	
R2 (See Note1)	0 to 27 Ω	Resistor, Chip, 0402, 5%, 1/16W	various	
R1	30 KΩ	Resistor, Chip, 0402, 5%, 1/16W	various	

Notes:

1. For Vcc1>4.5V, value of R2 may be varied between 0 and 27 Ohms for EVM floor optimization.

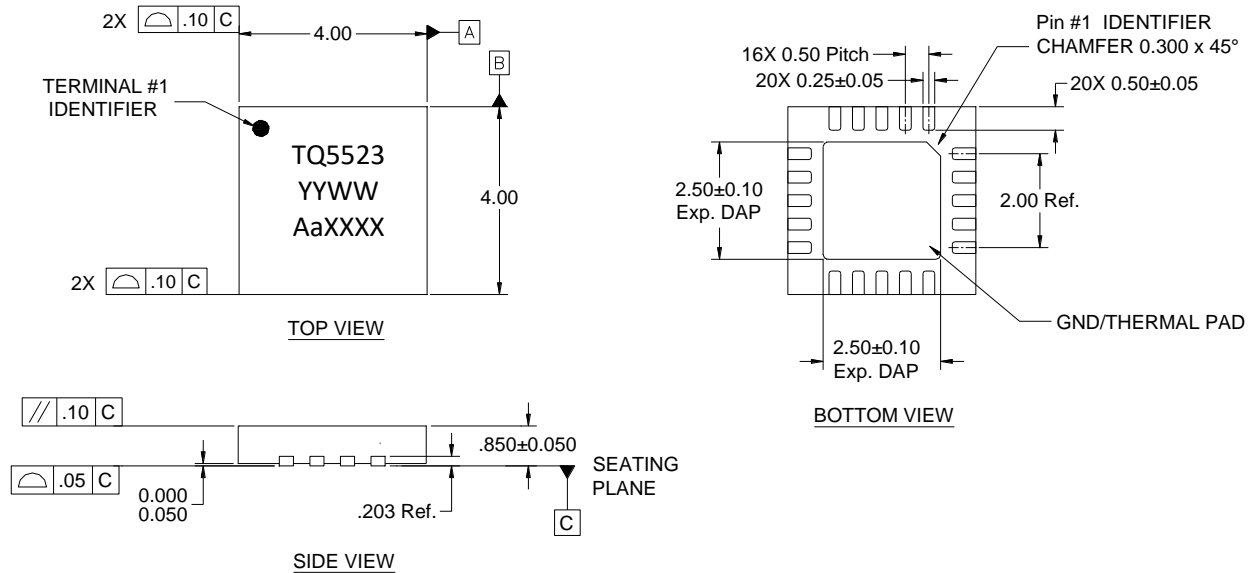
Pin Configuration and Description



Pin No.	Label	Description
1	NC	No internal connection. This pin can be grounded or N/C on PCB.
2	GND	Ground
3	RF_IN	RF Input. Internal DC Blocked
4	GND	Ground
5	PA_EN	PA Enable
6,7,8,9	NC	No internal connection. This pin can be grounded or N/C on PCB. Land pads should be provided for PCB mounting integrity.
10	DET	Detector Output
11	GND	Ground
12	GND	Ground
13	RF_OUT	RF Output. Internal DC Blocked
14	GND	Ground
15	GND	Ground
16	GND	Ground
17	GND	Ground
18	V _{CC3}	Supply voltage for third stage PA
19	V _{CC2}	Supply voltage for second stage PA
20	V _{CC1}	Supply voltage for first stage PA
Backside Pad	RF/DC GND	FEM RF/DC ground. Use recommended via pattern to minimize inductance and thermal resistance. See PCB Mounting Pattern for suggested footprint.

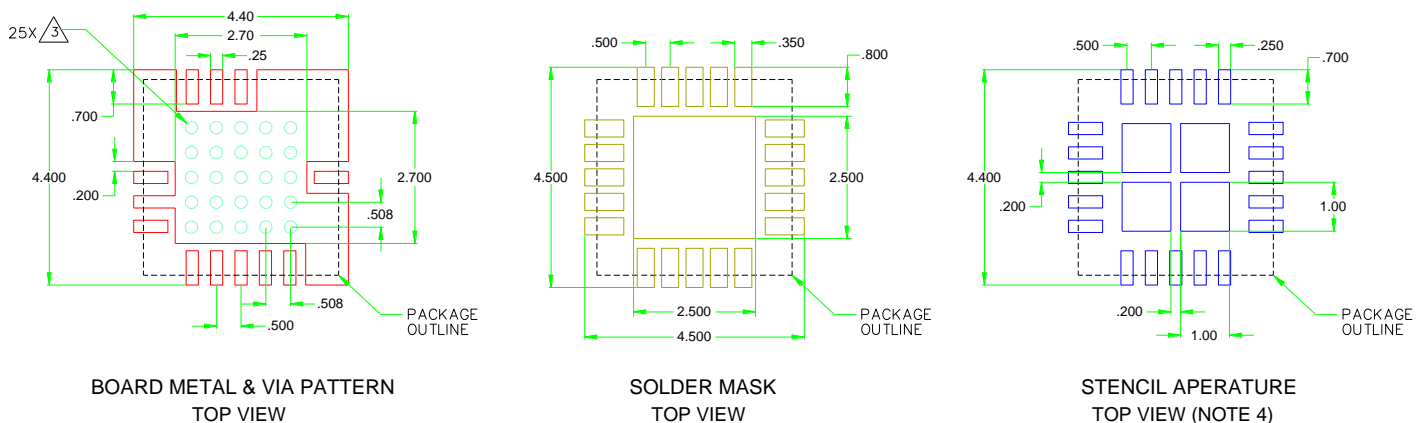
Package Marking and Dimensions

Marking: Product Identifier – “TQ5523”
 Date Code – YYWW
 Lot Code – aXXXX



- Notes:
1. All dimensions are in millimeters.
 2. Contact plating: NiPdAu.

PCB Mounting Pattern



- Notes:
1. All dimensions are in millimeters. Angles are in degrees.
 2. Use 1 oz. copper minimum for top and bottom layer metal.
 3. Vias are required under the backside paddle of this device for proper RF/DC grounding and thermal dissipation. We recommend a 0.35mm (#80/.0135") diameter bit for drilling via holes and a final plated thru diameter of 0.25 mm (0.10").
 4. Ensure good package backside paddle solder attach for reliable operation and best electrical performance.

Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class 1C	ESDA / JEDEC JS-001-2012
ESD – Charged Device Model (CDM)	Class C3	JEDEC JESD22-C101F
MSL – Moisture Sensitivity Level	Level 1	IPC/JEDEC J-STD-020



Caution!
ESD-Sensitive Device

Solderability

Compatible with both lead-free (260°C max. reflow temp.) and tin/lead (245°C max. reflow temp.) soldering processes. Solder profiles available upon request.

Contact plating: NiPdAu

RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A (C₁₅H₁₂Br₄O₂) Free
- PFOS Free
- SVHC Free



Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

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Email: customer.support@qorvo.com

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