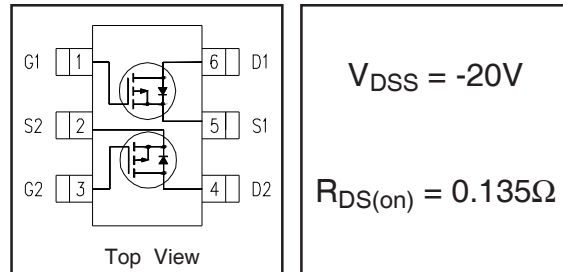


IRF5850PbF

HEXFET® Power MOSFET

- Ultra Low On-Resistance
- Dual P-Channel MOSFET
- Surface Mount
- Available in Tape & Reel
- Low Gate Charge
- Lead-Free
- Halogen-Free



Description

These P-channel MOSFETs from International Rectifier utilize advanced processing techniques to achieve the extremely low on-resistance per silicon area. This benefit provides the designer with an extremely efficient device for use in battery and load management applications.

This Dual TSOP-6 package is ideal for applications where printed circuit board space is at a premium and where maximum functionality is required. With two die per package, the IRF5850 can provide the functionality of two SOT-23 packages in a smaller footprint. Its unique thermal design and $R_{DS(on)}$ reduction enables an increase in current-handling capability.



Absolute Maximum Ratings

	Parameter	Max.	Units
V_{DS}	Drain- Source Voltage	-20	V
$I_D @ T_A = 25^\circ C$	Continuous Drain Current, $V_{GS} @ -4.5V$	-2.2	A
$I_D @ T_A = 70^\circ C$	Continuous Drain Current, $V_{GS} @ -4.5V$	-1.8	
I_{DM}	Pulsed Drain Current ①	-9.0	
$P_D @ T_A = 25^\circ C$	Power Dissipation	0.96	W
$P_D @ T_A = 70^\circ C$	Power Dissipation	0.62	
	Linear Derating Factor	7.7	mW/°C
V_{GS}	Gate-to-Source Voltage	± 12	V
T_J, T_{STG}	Junction and Storage Temperature Range	-55 to + 150	°C

Thermal Resistance

	Parameter	Max.	Units
$R_{\theta JA}$	Maximum Junction-to-Ambient③	130	°C/W

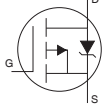
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Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	-20	—	—	V	$V_{GS} = 0V, I_D = -250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.011	—	V/ $^\circ\text{C}$	Reference to 25°C , $I_D = -1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.135	Ω	$V_{GS} = -4.5V, I_D = -2.2A$ ②
		—	—	0.220		$V_{GS} = -2.5V, I_D = -1.9A$ ②
$V_{GS(th)}$	Gate Threshold Voltage	-0.45	—	-1.2	V	$V_{DS} = V_{GS}, I_D = -250\mu A$
g_{fs}	Forward Transconductance	3.5	—	—	S	$V_{DS} = -10V, I_D = -2.2A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	-1.0	μA	$V_{DS} = -16V, V_{GS} = 0V$
		—	—	-25		$V_{DS} = -16V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	-100	nA	$V_{GS} = -12V$
	Gate-to-Source Reverse Leakage	—	—	100		$V_{GS} = 12V$
Q_g	Total Gate Charge	—	3.6	5.4	nC	$I_D = -2.2A$
Q_{gs}	Gate-to-Source Charge	—	0.66	—		$V_{DS} = -10V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	0.83	—		$V_{GS} = -4.5V$ ②
$t_{d(on)}$	Turn-On Delay Time	—	8.3	—	ns	$V_{DD} = -10V$ ②
t_r	Rise Time	—	14	—		$I_D = -1.0A$
$t_{d(off)}$	Turn-Off Delay Time	—	31	—		$R_G = 6.0\Omega$
t_f	Fall Time	—	28	—		$V_{GS} = -4.5V$
C_{iss}	Input Capacitance	—	320	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	56	—		$V_{DS} = -15V$
C_{rss}	Reverse Transfer Capacitance	—	40	—		$f = 1.0\text{kHz}$

Source-Drain Ratings and Characteristics

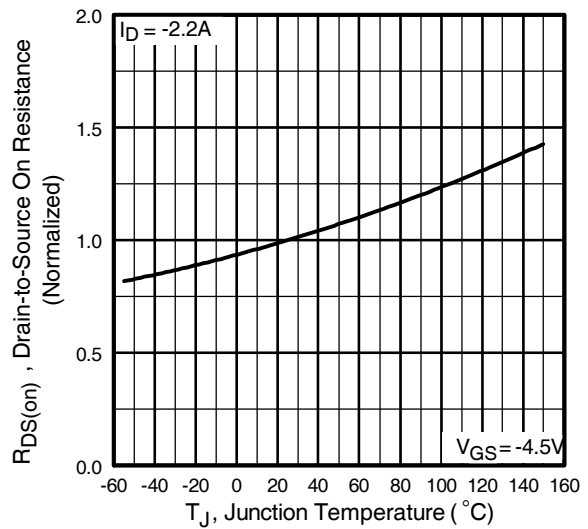
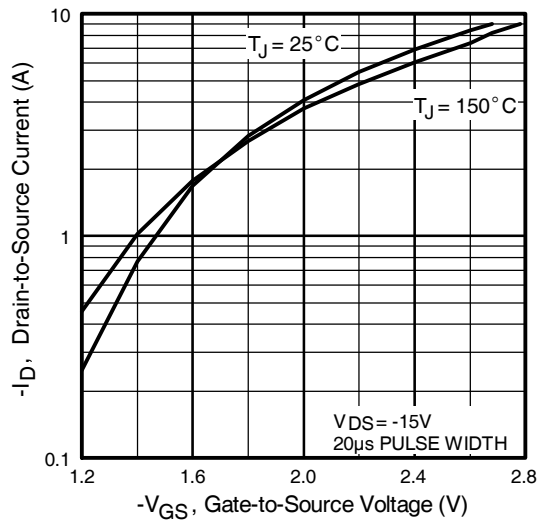
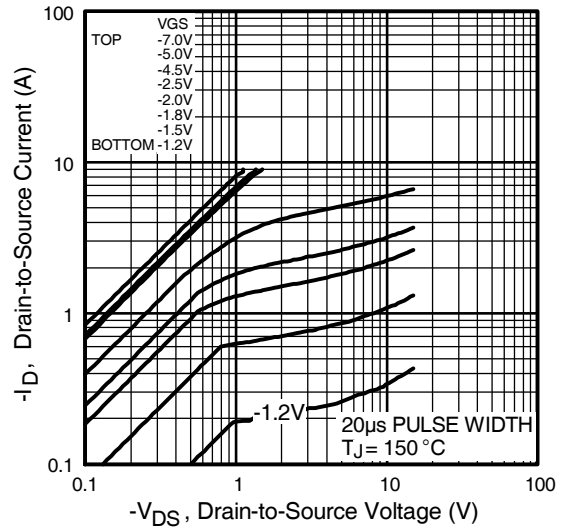
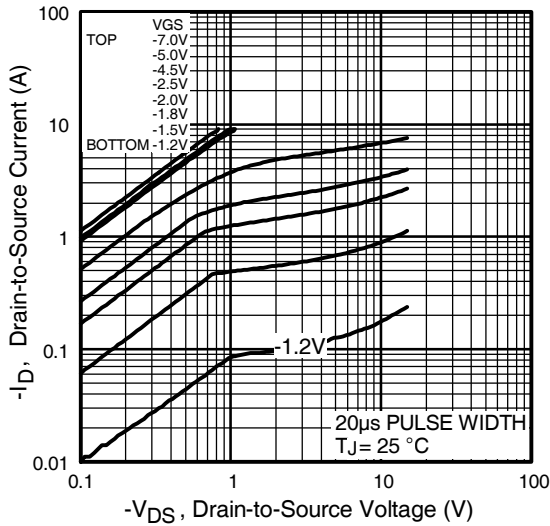
	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	-0.96	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	-9.0		
V_{SD}	Diode Forward Voltage	—	—	-1.2	V	$T_J = 25^\circ\text{C}, I_S = -0.96A, V_{GS} = 0V$ ②
t_{rr}	Reverse Recovery Time	—	23	35	ns	$T_J = 25^\circ\text{C}, I_F = -0.96A$
Q_{rr}	Reverse Recovery Charge	—	7.7	12	nC	$di/dt = -100A/\mu s$ ②

Notes:

① Repetitive rating; pulse width limited by max. junction temperature.

③ Surface mounted on FR-4 board, $t \leq 5\text{sec}$.

② Pulse width $\leq 400\mu s$; duty cycle $\leq 2\%$.



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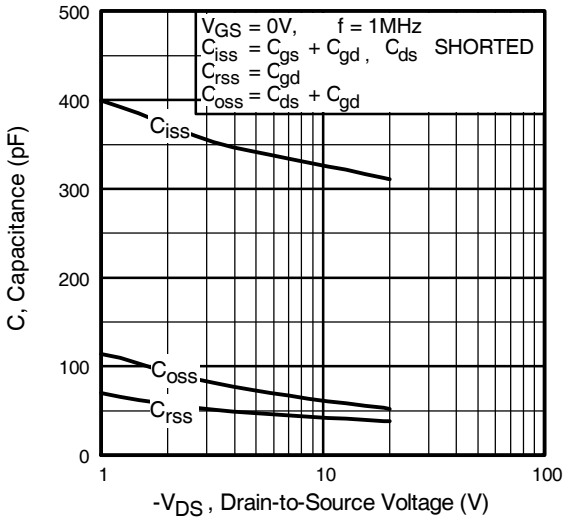


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

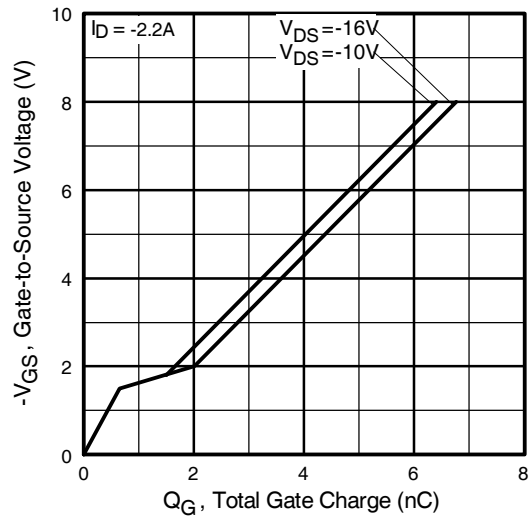


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

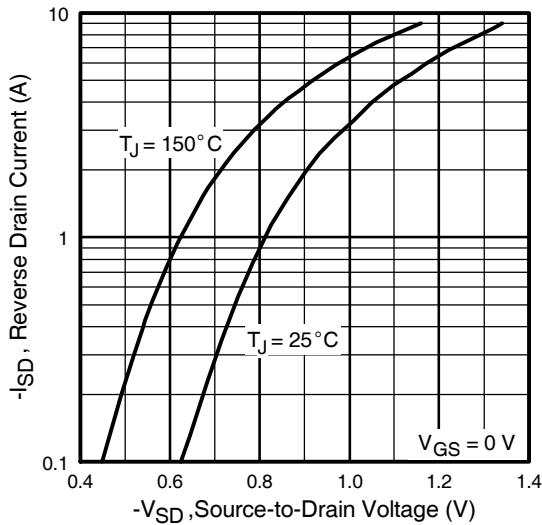


Fig 7. Typical Source-Drain Diode Forward Voltage

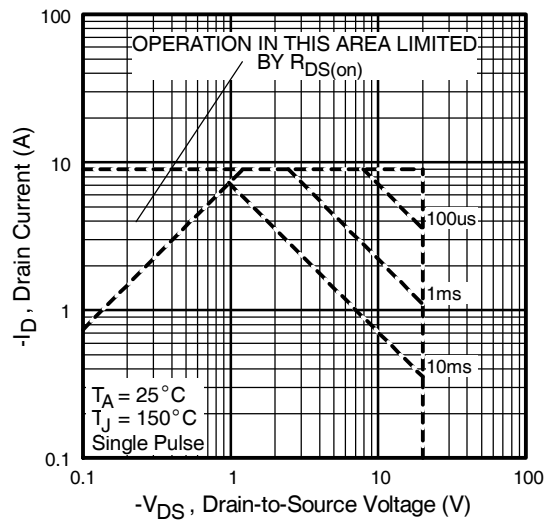


Fig 8. Maximum Safe Operating Area

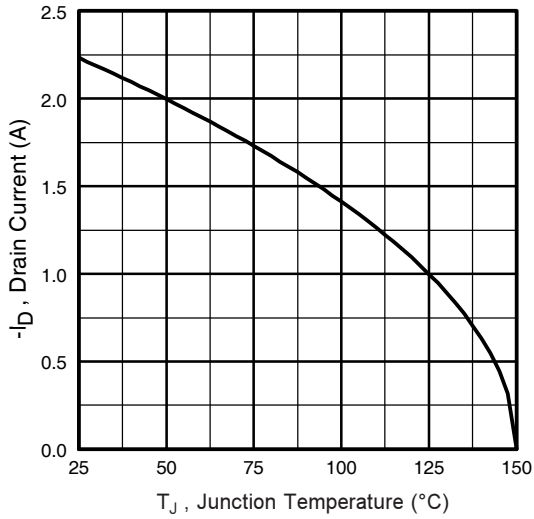


Fig 9. Maximum Drain Current Vs. Junction Temperature

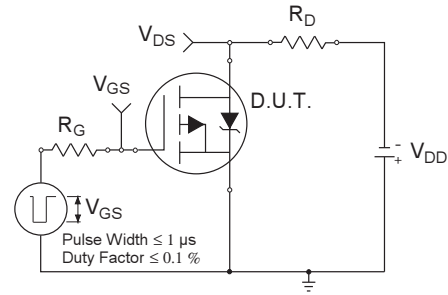


Fig 10a. Switching Time Test Circuit

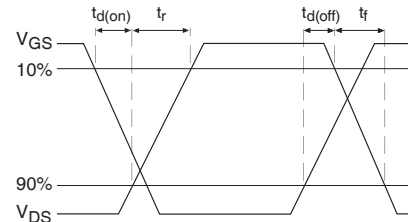


Fig 10b. Switching Time Waveforms

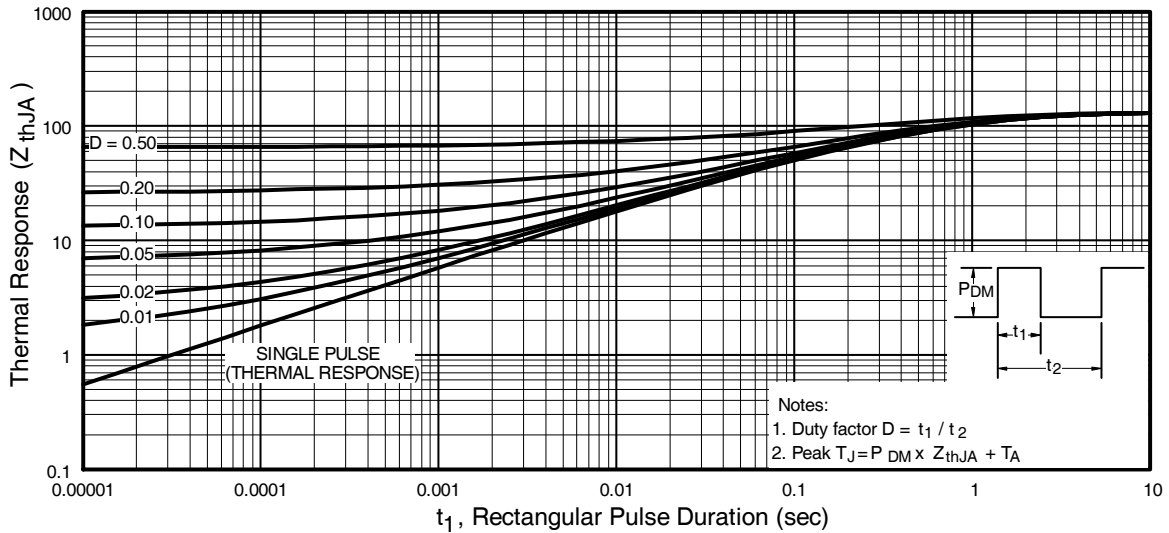


Fig 10. Typical Effective Transient Thermal Impedance, Junction-to-Ambient

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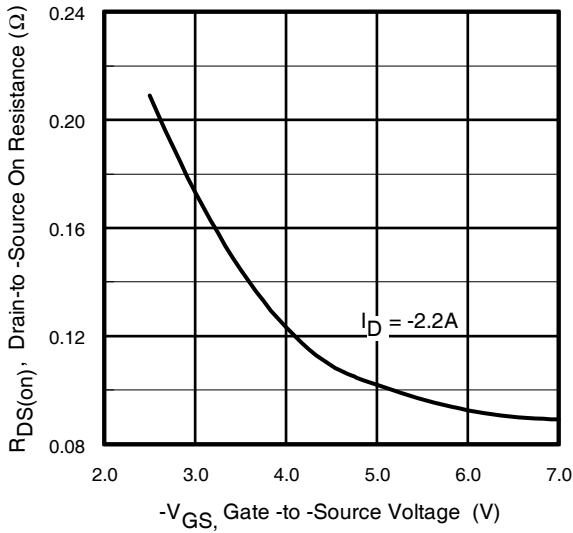


Fig 11. Typical On-Resistance Vs. Gate Voltage

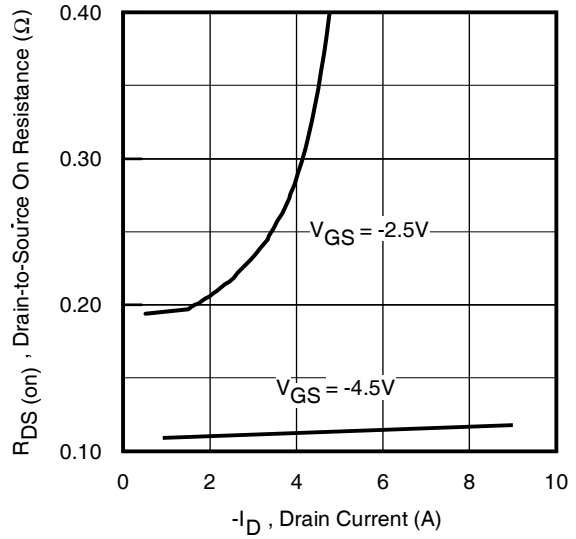


Fig 12. Typical On-Resistance Vs. Drain Current

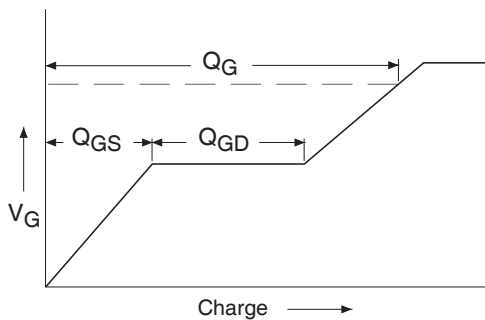


Fig 13a. Basic Gate Charge Waveform

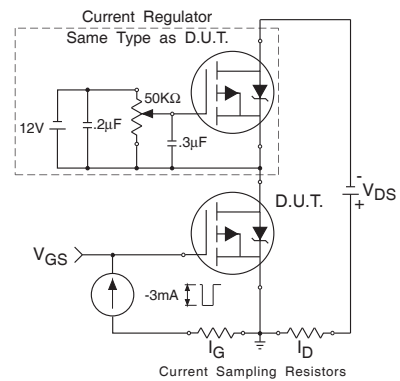


Fig 13b. Gate Charge Test Circuit

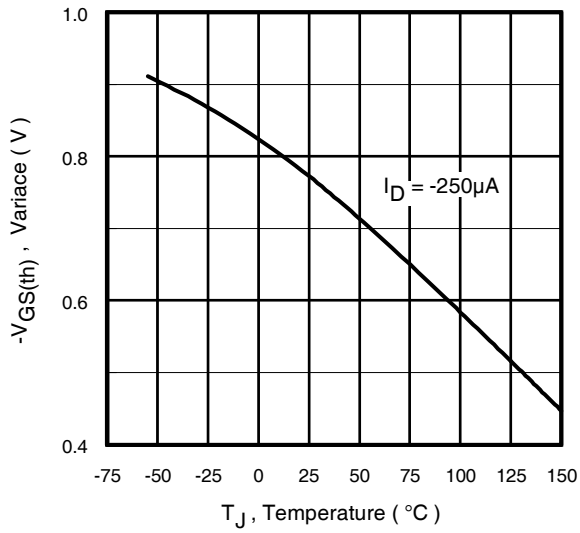


Fig 14. Threshold Voltage Vs. Temperature

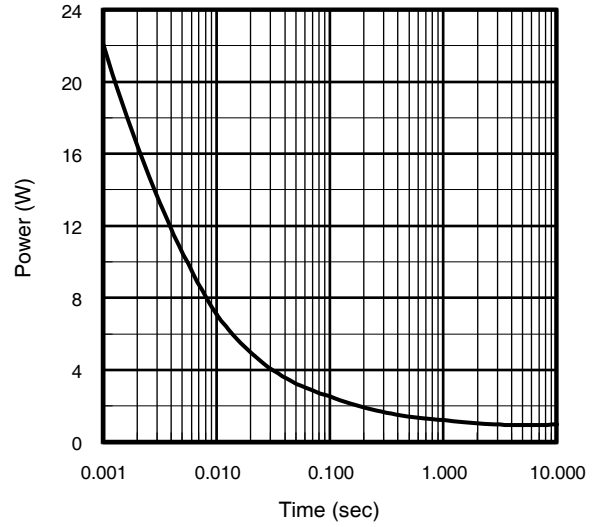
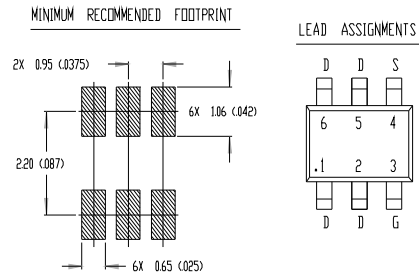
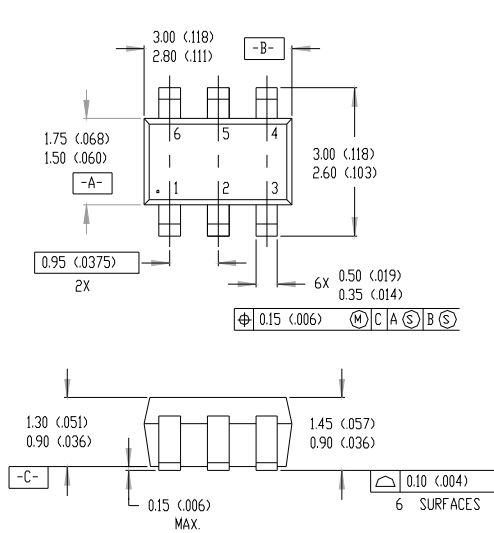


Fig 15. Typical Power Vs. Time

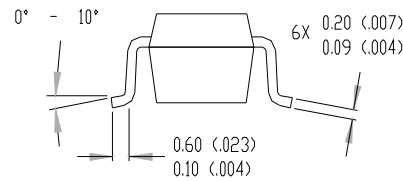
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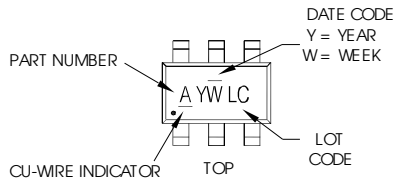
TSOP-6 Package Outline



- NOTES:
 1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).



TSOP-6 Part Marking Information



PART NUMBER CODE REFERENCE:

- A = SI3443DV K = IRF5810
 B = IRF5800 L = IRF5804
 C = IRF5850 M = IRF5803
 D = IRF5851 N = IRF5802
 E = IRF5852
 F = IRF5801
 I = IRF5805
 J = IRF5806

- Notes:
 -A line above the work week (as shown here) indicates Lead-Free
 -A line below the part number (as shown here) indicates Cu-wire

W = (1-26) IF PRECEDED BY LAST DIGIT OF CALENDAR YEAR

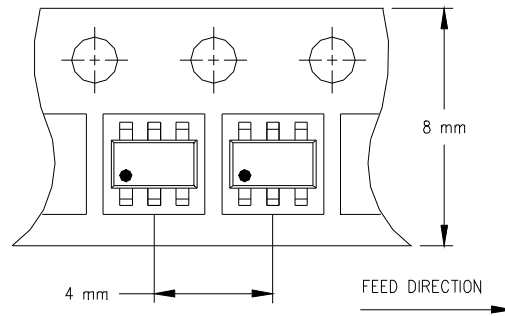
YEAR	Y	WORK WEEK	W
2001	1	01	A
2002	2	02	B
2003	3	03	C
2004	4	04	D
2005	5		
2006	6		
2007	7		
2008	8		
2009	9		
2010	0	24	X
		25	Y
		26	Z

W = (27-52) IF PRECEDED BY A LETTER

YEAR	Y	WORK WEEK	W
2001	A	27	A
2002	B	28	B
2003	C	29	C
2004	D	30	D
2005	E		
2006	F		
2007	G		
2008	H		
2009	J		
2010	K	50	X
		51	Y
		52	Z

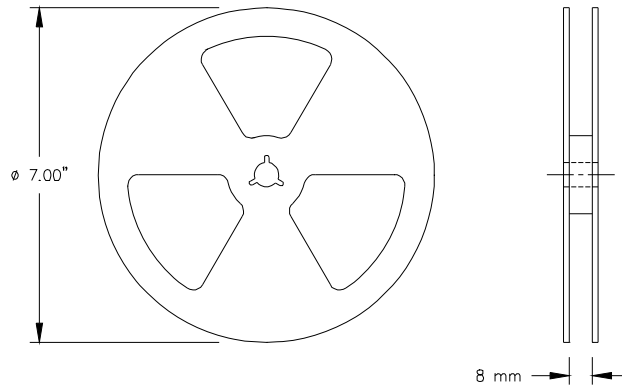
Note: For the most current drawing please refer to IR website at: <http://www.irf.com/package/>

TSOP-6 Tape & Reel Information



NOTES:

1. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES:

1. OUTLINE CONFORMS TO EIA-481 & EIA-541.

Data and specifications subject to change without notice.
This product has been designed and qualified for the Consumer market.
Qualifications Standards can be found on IR's Web site.

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TAC Fax: (310) 252-7903

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