High Performance
128K×8
CMOS SRAM

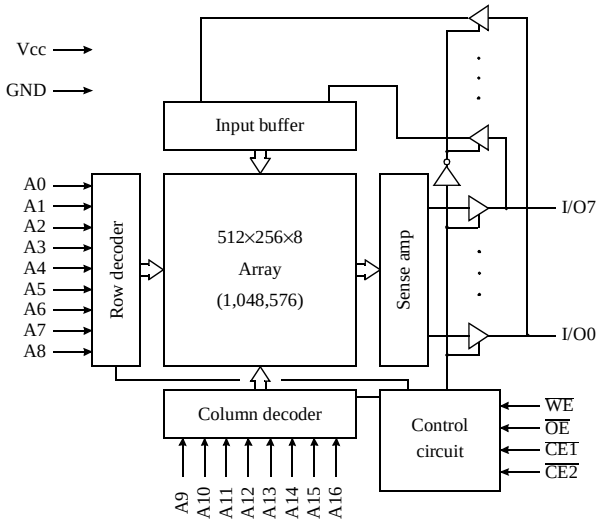
AS7C1024
AS7C31024

128K×8 CMOS SRAM

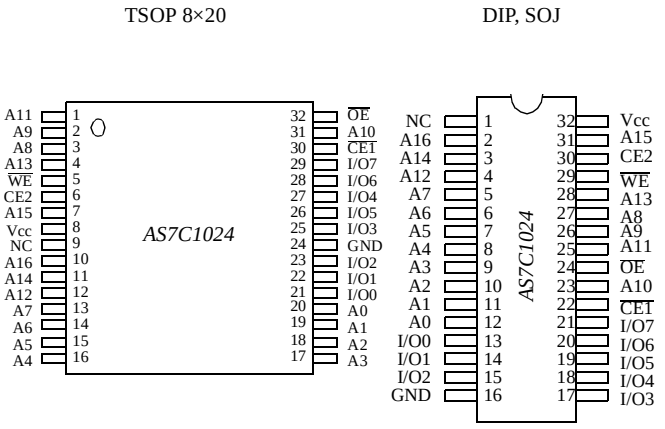
## Features

- Organization: 131,072 words × 8 bits
- High speed
  - 10/12/15/20 ns address access time
  - 3/3/4/5 ns output enable access time
- Low power consumption
  - Active: 660 mW max (15 ns cycle)
  - Standby: 55 mW max, CMOS I/O
  - Very low DC component in active power
- 2.0V data retention
- Equal access and cycle times
- Easy memory expansion with $\overline{CE1}$, CE2, $\overline{OE}$ inputs
- TTL/LVTTL-compatible, three-state I/O
- 32-pin JEDEC standard packages
  - 300 mil PDIP and SOJ
    Socket compatible with 7C512 (64K×8)
  - 400 mil PDIP and SOJ
  - 8×20 TSOP
- ESD protection ≥ 2000 volts
- Latch-up current ≥ 200 mA
- 3.3V and 5.0V versions available
- Industrial and commercial temperature available

## Logic block diagram




## Pin arrangement




## Selection guide

| | | 7C1024-10<br>– | 7C1024-12<br>7C31024-12 | 7C1024-15<br>7C31024-15 | 7C1024-20<br>7C31024-20 | Unit |
|---|---|---|---|---|---|---|
| Maximum address access time | | 10 | 12 | 15 | 20 | ns |
| Maximum output enable access time | | 3 | 3 | 4 | 5 | ns |
| Maximum operating current | AS7C1024 | 175 | 160 | 120 | 110 | mA |
| | AS7C31024 | – | 100 | 70 | 65 | mA |
| Maximum CMOS standby current | | 10.0 | 10.0 | 10.0 | 10.0 | mA |

Shaded areas contain advance information.



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## Functional description

The AS7C1024 and AS7C31024 are high performance CMOS 1,048,576-bit Static Random Access Memories (SRAM) organized as 131,072 words × 8 bits. It is designed for memory applications where fast data access, low power, and simple interfacing are desired.

Equal address access and cycle times ($t_{AA}$, $t_{RC}$, $t_{WC}$) of 10/12/15/20 ns with output enable access times ($t_{OE}$) of 3/3/4/5 ns are ideal for high performance applications. Active high and low chip enables ($\overline{CE1}$, CE2) permit easy memory expansion with multiple-bank memory systems.

When $\overline{CE1}$ is HIGH or CE2 is LOW the device enters standby mode. The standard AS7C1024 is guaranteed not to exceed 55 mW power consumption in standby mode. Both devices offer 2.0V data retention.

A write cycle is accomplished by asserting write enable ($\overline{WE}$) and both chip enables ($\overline{CE1}$, CE2). Data on the input pins I/O0-I/O7 is written on the rising edge of $\overline{WE}$ (write cycle 1) or the active-to-inactive edge of $\overline{CE1}$ or CE2 (write cycle 2). To avoid bus contention, external devices should drive I/O pins only after outputs have been disabled with output enable ($\overline{OE}$) or write enable ($\overline{WE}$).

A read cycle is accomplished by asserting output enable ($\overline{OE}$) and both chip enables ($\overline{CE1}$, CE2), with write enable ($\overline{WE}$) HIGH. The chip drives I/O pins with the data word referenced by the input address. When either chip enable or output enable is inactive, or write enable is active, output drivers stay in high-impedance mode.

All chip inputs and outputs are TTL/LVTTL-compatible, and operation is from a single 5V supply (AS7C1024) or 3.3V supply (AS7C31024). The AS7C1024 and AS7C31024 are packaged in common industry standard packages.

## Absolute maximum ratings

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Voltage on any pin relative to GND | $V_t$ | −0.5 | +7.0 | V |
| Power dissipation | $P_D$ | – | 1.0 | W |
| Storage temperature (plastic) | $T_{stg}$ | −55 | +150 | °C |
| Temperature under bias | $T_{bias}$ | −10 | +85 | °C |
| DC output current | $I_{out}$ | – | 20 | mA |

Stresses greater than those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## Truth table

| $\overline{CE1}$ | CE2 | $\overline{WE}$ | $\overline{OE}$ | Data | Mode |
|---|---|---|---|---|---|
| H | X | X | X | High Z | Standby ($I_{SB}$, $I_{SB1}$) |
| X | L | X | X | High Z | Standby ($I_{SB}$, $I_{SB1}$) |
| L | H | H | H | High Z | Output disable |
| L | H | H | L | $D_{out}$ | Read |
| L | H | L | X | $D_{in}$ | Write |

Key: X = Don't Care, L = LOW, H = HIGH

## Recommended operating conditions

| Parameter | | Symbol | Min | Nominal | Max | Unit |
|---|---|---|---|---|---|---|
| Supply voltage | AS7C1024 | $V_{CC}$ | 4.5 | 5.0 | 5.5 | V |
| | AS7C31024 | $V_{CC}$ | 3.0 | 3.3 | 3.6 | V |
| | | GND | 0.0 | 0.0 | 0.0 | V |
| Input voltage | AS7C1024 | $V_{IH}$ | 2.2 | – | $V_{CC}$ + 0.5 | V |
| | AS7C31024 | $V_{IH}$ | 2.0 | – | $V_{CC}$ + 0.5 | V |
| | | $V_{IL}$ | −0.5 | – | 0.8 | V |

†$V_{IL}$ min = −3.0V for pulse width less than $t_{RC}/2$.

## DC operating characteristics [1]

| Parameter | Symbol | Test conditions | | -10 Min | -10 Max | -12 Min | -12 Max | -15 Min | -15 Max | -20 Min | -20 Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Input leakage current | $\lvert I_{LI} \rvert$ | $V_{CC}$ = Max, $V_{in}$ = GND to $V_{CC}$ | | – | 1 | – | 1 | – | 1 | – | 1 | µA |
| Output leakage current | $\lvert I_{LO} \rvert$ | $\overline{CE1}$ = $V_{IH}$ or CE2 = $V_{IL}$, $V_{CC}$ = Max, $V_{out}$ = GND to $V_{CC}$ | | – | 1 | – | 1 | – | 1 | – | 1 | µA |
| Operating power supply current | $I_{CC}$ | $\overline{CE1}$ = $V_{IL}$, CE2 = $V_{IH}$, f = $f_{max}$, $I_{out}$ = 0 mA | AS7C1024 | – | 175 | – | 160 | – | 120 | – | 110 | mA |
| | | | AS7C31024 | – | – | – | 100 | – | 70 | – | 65 | mA |
| Standby power supply current | $I_{SB}$ | $\overline{CE1}$ = $V_{IH}$ or CE2 = $V_{IL}$, f = $f_{max}$ | | – | 55 | – | 50 | – | 40 | – | 40 | mA |
| | $I_{SB1}$ | $\overline{CE1}$ ≥ $V_{CC}$–0.2V or CE2 ≤0.2V, $V_{in}$ ≤ 0.2V or $V_{in}$ ≥ $V_{CC}$–0.2V, f = 0 | | – | 10 | – | 10 | – | 10 | – | 10 | mA |
| Output voltage | $V_{OL}$ | $I_{OL}$ = 8 mA, $V_{CC}$ = Min | | – | 0.4 | – | 0.4 | – | 0.4 | – | 0.4 | V |
| | $V_{OH}$ | $I_{OH}$ = –4 mA, $V_{CC}$ = Min | | 2.4 | – | 2.4 | – | 2.4 | – | 2.4 | – | V |

Shaded areas contain advance information.

## Capacitance [2]

(f = 1 MHz, $T_a$ = Room temperature, $V_{CC}$ = 5V)

| Parameter | Symbol | Signals | Test conditions | Max | Unit |
|---|---|---|---|---|---|
| Input capacitance | $C_{IN}$ | A, $\overline{CE1}$, CE2, $\overline{WE}$, $\overline{OE}$ | $V_{in}$ = 0V | 5 | pF |
| I/O capacitance | $C_{I/O}$ | I/O | $V_{in}$ = $V_{out}$ = 0V | 7 | pF |

## Read cycle [3,9,12]

| Parameter | Symbol | -10 Min | -10 Max | -12 Min | -12 Max | -15 Min | -15 Max | -20 Min | -20 Max | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Read cycle time | $t_{RC}$ | 10 | – | 12 | – | 15 | – | 20 | – | ns | |
| Address access time | $t_{AA}$ | – | 10 | – | 12 | – | 15 | – | 20 | ns | 3 |
| Chip enable ($\overline{CE1}$) access time | $t_{ACE1}$ | – | 10 | – | 12 | – | 15 | – | 20 | ns | 3, 12 |
| Chip enable (CE2) access time | $t_{ACE2}$ | – | 10 | – | 12 | – | 15 | – | 20 | ns | 3, 12 |
| Output enable ($\overline{OE}$) access time | $t_{OE}$ | – | 3 | – | 3 | – | 4 | – | 5 | ns | |
| Output hold from address change | $t_{OH}$ | 2 | – | 3 | – | 3 | – | 3 | – | ns | 5 |
| $\overline{CE1}$ LOW to output in Low Z | $t_{CLZ1}$ | 3 | – | 3 | – | 3 | – | 3 | – | ns | 4, 5, 12 |
| CE2 HIGH to output in Low Z | $t_{CLZ2}$ | 3 | – | 3 | – | 3 | – | 3 | – | ns | 4, 5, 12 |
| $\overline{CE1}$ HIGH to output in High Z | $t_{CHZ1}$ | – | 3 | – | 3 | – | 4 | – | 5 | ns | 4, 5, 12 |
| CE2 LOW to output in High Z | $t_{CHZ2}$ | – | 3 | – | 3 | – | 4 | – | 5 | ns | 4, 5, 12 |
| $\overline{OE}$ LOW to output in Low Z | $t_{OLZ}$ | 0 | – | 0 | – | 0 | – | 0 | – | ns | 4, 5 |
| $\overline{OE}$ HIGH to output in High Z | $t_{OHZ}$ | – | 3 | – | 3 | – | 4 | – | 5 | ns | 4, 5 |
| Power up time | $t_{PU}$ | 0 | – | 0 | – | 0 | – | 0 | – | ns | 4, 5, 12 |
| Power down time | $t_{PD}$ | – | 10 | – | 12 | – | 15 | – | 20 | ns | 4, 5, 12 |



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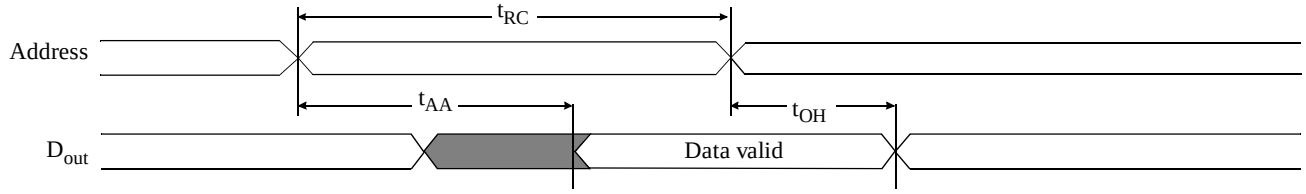
## Key to switching waveforms

Rising input  Falling input  Undefined output/don't care

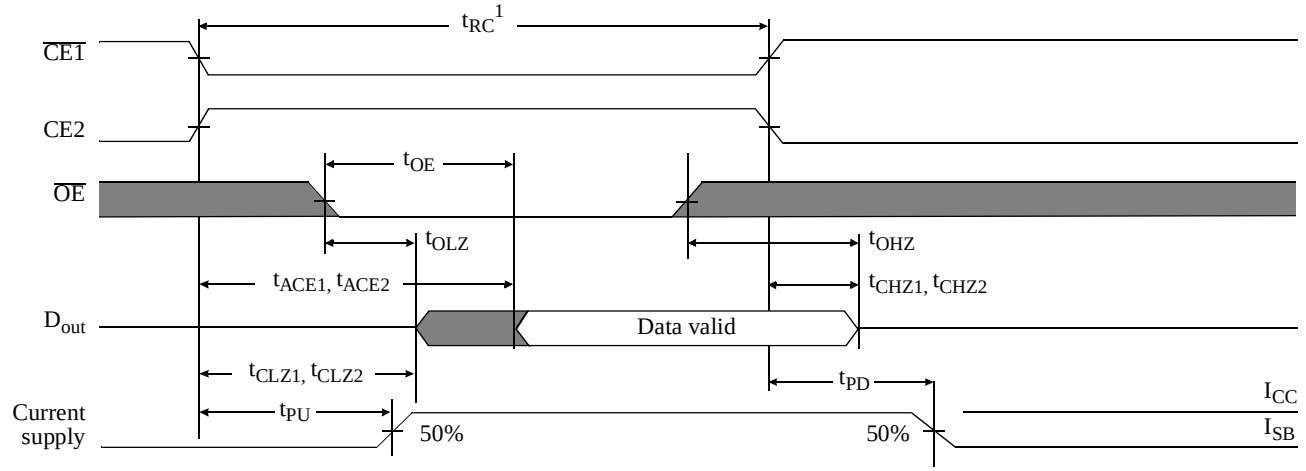
## Read waveform 1 [3,6,7,9,12]

Address controlled




## Read waveform 2 [3,6,8,9,12]

$\overline{CE1}$ and CE2 controlled



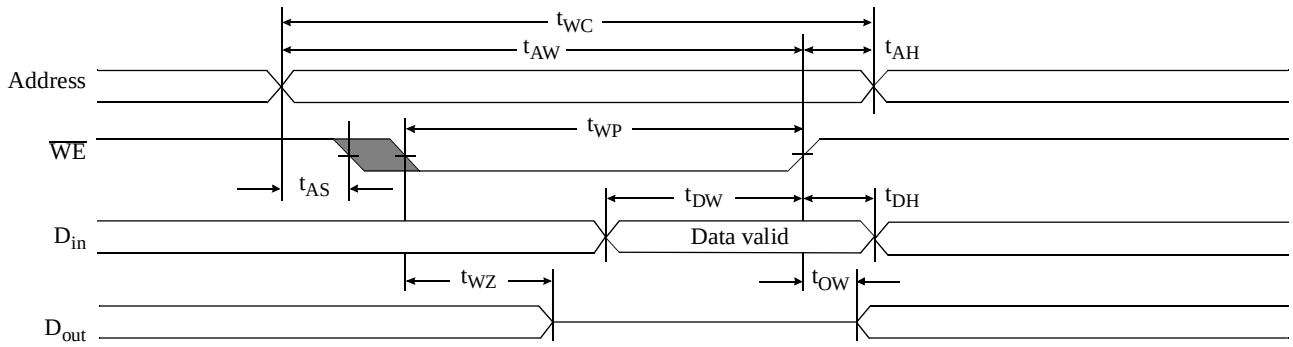

## Write cycle [11, 12]

| | | -10 | | -12 | | -15 | | -20 | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Parameter | Symbol | Min | Max | Min | Max | Min | Max | Min | Max | Unit | Notes |
| Write cycle time | $t_{WC}$ | 10 | – | 12 | – | 15 | – | 20 | – | ns | |
| Chip enable ($\overline{CE1}$) to write end | $t_{CW1}$ | 9 | – | 10 | – | 12 | – | 12 | – | ns | 12 |
| Chip enable (CE2) to write end | $t_{CW2}$ | 9 | – | 10 | – | 12 | – | 12 | – | ns | 12 |
| Address setup to write end | $t_{AW}$ | 9 | – | 10 | – | 12 | – | 12 | – | ns | |
| Address setup time | $t_{AS}$ | 0 | – | 0 | – | 0 | – | 0 | – | ns | 12 |
| Write pulse width | $t_{WP}$ | 7 | – | 8 | – | 9 | – | 12 | – | ns | |
| Address hold from end of write | $t_{AH}$ | 0 | – | 0 | – | 0 | – | 0 | – | ns | |
| Data valid to write end | $t_{DW}$ | 6 | – | 6 | – | 9 | – | 10 | – | ns | |
| Data hold time | $t_{DH}$ | 0 | – | 0 | – | 0 | – | 0 | – | ns | 4, 5 |
| Write enable to output in High Z | $t_{WZ}$ | – | 5 | – | 5 | – | 5 | – | 5 | ns | 4, 5 |
| Output active from write end | $t_{OW}$ | 3 | – | 3 | – | 3 | – | 3 | – | ns | 4, 5 |

Shaded areas contain advance information.

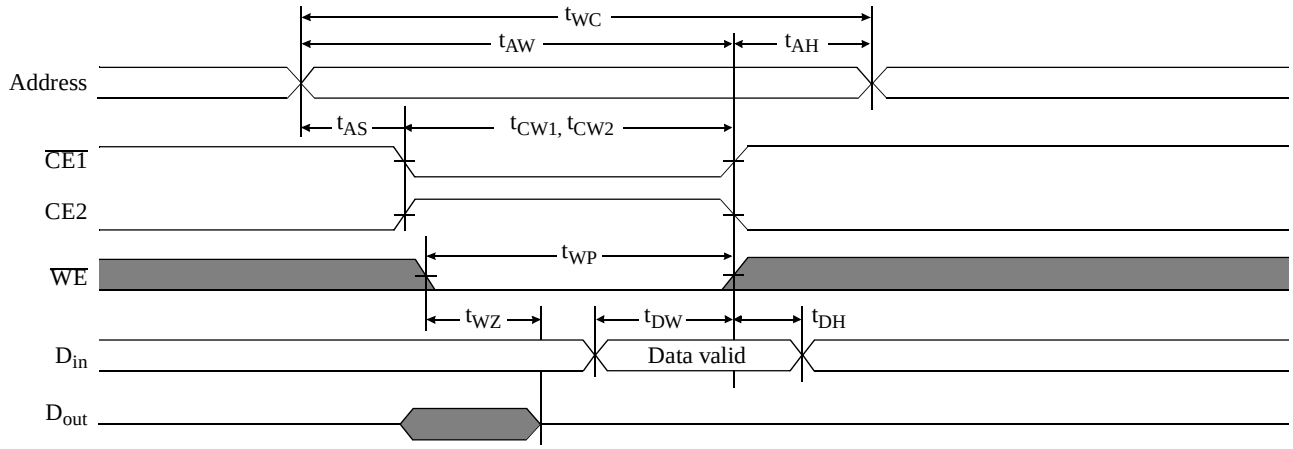
## Write waveform 1 [10,11,12]

$\overline{WE}$ controlled




## Write waveform 2 [10,11,12]

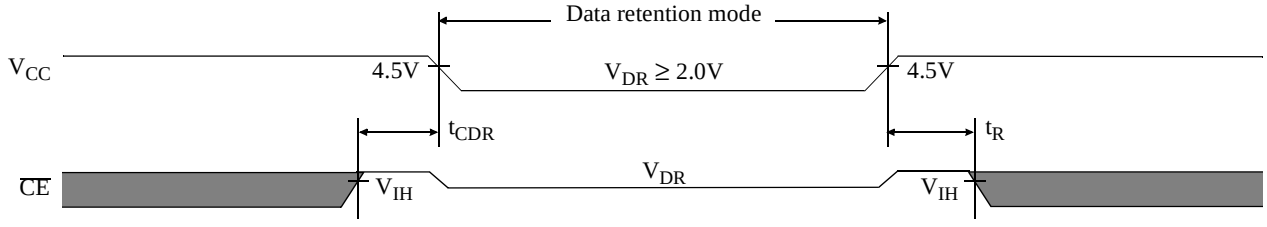
$\overline{CE1}$ and CE2 controlled




## Data retention characteristics [14]

| Parameter | Symbol | Test conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ for data retention | $V_{DR}$ | $V_{CC}$ = 2.0V | 2.0 | – | V |
| Data retention current | $I_{CCDR}$ | $\overline{CE1} \geq V_{CC}-0.2V$ or | – | 500 | µA |
| Chip deselect to data retention time | $t_{CDR}$ | CE2 ≤ 0.2V | 0 | – | ns |
| Operation recovery time | $t_R$ | $V_{in} \geq V_{CC}-0.2V$ or | $t_{RC}$ | – | ns |
| Input leakage current | $\lvert I_{LI} \rvert$ | $V_{in} \leq 0.2V$ | – | 1 | µA |

## Data retention waveform



## AC test conditions

- 5V output load: see Figure B, except as noted see Figure C.
- 3.3V output load: see Figure D, except as noted see Figure E.
- Input pulse level: GND to 3.0V. See Figure A.
- Input rise and fall times: 5 ns. See Figure A.
- Input and output timing reference levels: 1.5V.

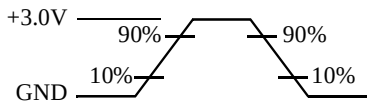



Figure A: Input waveform

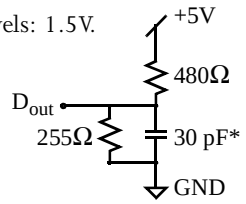
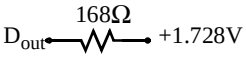



Figure B: Output load

Thevenin equivalent:



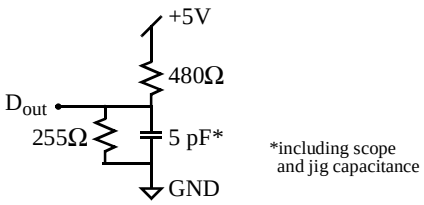




Figure C: Output load for $t_{CLZ}$, $t_{CHZ}$, $t_{OLZ}$, $t_{OHZ}$, $t_{OW}$

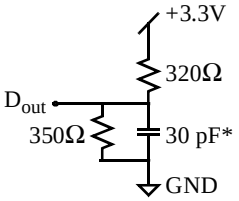



Figure D: Output load

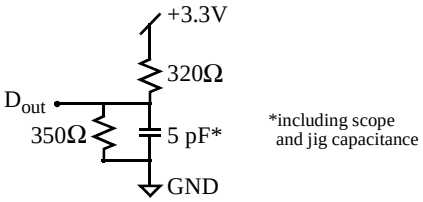


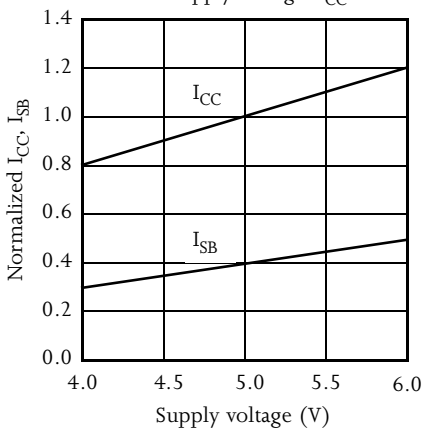

Figure C: Output load for $t_{CLZ}$, $t_{CHZ}$, $t_{OLZ}$, $t_{OHZ}$, $t_{OW}$

## Notes

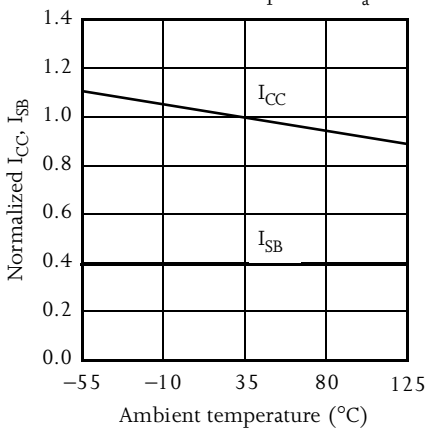
1 During $V_{CC}$ power-up, a pull-up resistor to $V_{CC}$ on $\overline{CE1}$ is required to meet $I_{SB}$ specification.
2 This parameter is sampled and not 100% tested.
3 For test conditions, see *AC Test Conditions*, Figures A, B, C.
4 $t_{CLZ}$ and $t_{CHZ}$ are specified with CL = 5pF as in Figure C. Transition is measured ±500mV from steady-state voltage.
5 This parameter is guaranteed but not tested.
6 $\overline{WE}$ is HIGH for read cycle.
7 $\overline{CE1}$ and $\overline{OE}$ are LOW and CE2 is HIGH for read cycle.
8 Address valid prior to or coincident with $\overline{CE}$ transition LOW.
9 All read cycle timings are referenced from the last valid address to the first transitioning address.
10 $\overline{CE1}$ or $\overline{WE}$ must be HIGH or CE2 LOW during address transitions.
11 All write cycle timings are referenced from the last valid address to the first transitioning address.
12 $\overline{CE1}$ and CE2 have identical timing.
13 This data applicable to the AS7C1024. The AS7C31024 functions similarly.
14 2V data retention applies to commercial tempoerature operating range only.

## *Typical DC and AC characteristics*

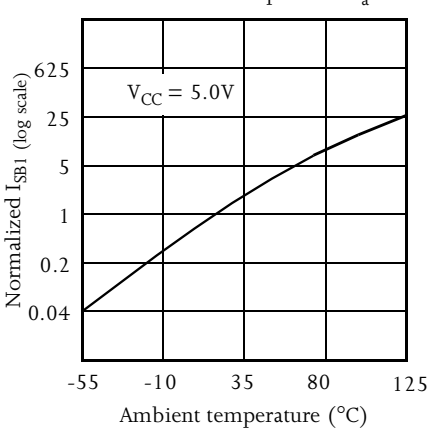
Normalized supply current $I_{CC}$, $I_{SB}$ vs. supply voltage $V_{CC}$



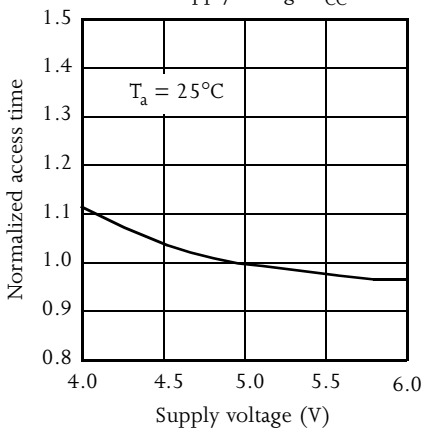

Normalized supply current $I_{CC}$, $I_{SB}$ vs. ambient temperature $T_a$



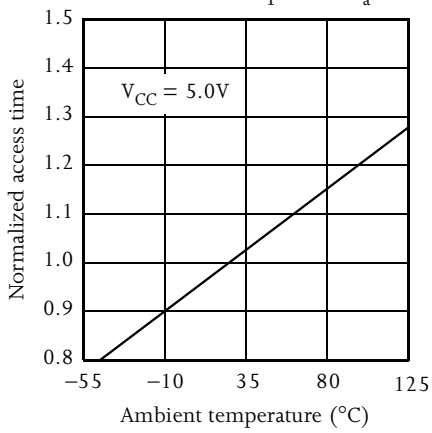

Normalized supply current $I_{SB1}$ vs. ambient temperature $T_a$



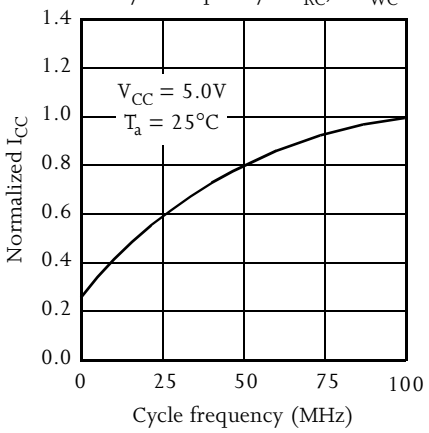

Normalized access time $t_{AA}$ vs. supply voltage $V_{CC}$



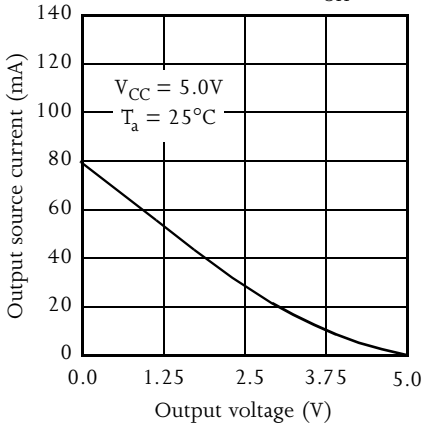

Normalized access time $t_{AA}$ vs. ambient temperature $T_a$



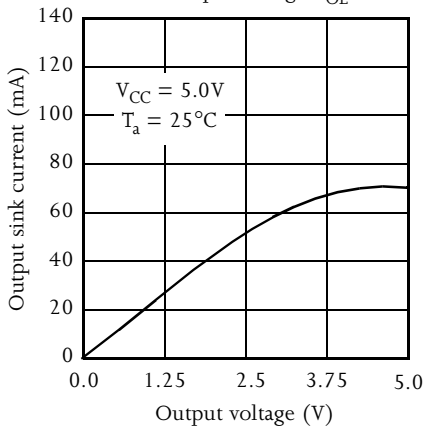

Normalized supply current $I_{CC}$ vs. cycle frequency $1/t_{RC}$, $1/t_{WC}$



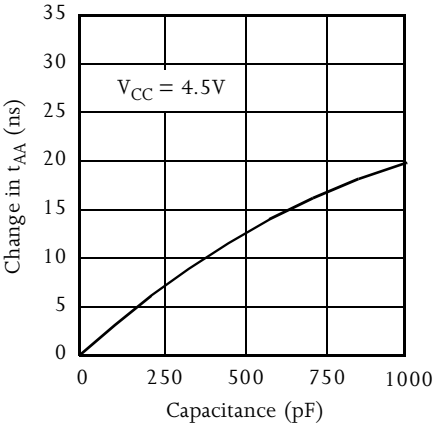

Output source current $I_{OH}$ vs. output voltage $V_{OH}$




Output sink current $I_{OL}$ vs. output voltage $V_{OL}$




Typical access time change $\Delta t_{AA}$ vs. output capacitive loading



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## AS7C1024 ordering codes

| Package \ Access time | 10 ns | 12 ns | 15 ns | 20 ns |
|---|---|---|---|---|
| Plastic DIP, 300 mil | | AS7C1024-12TPC<br>AS7C31024-12TPC | AS7C1024-15TPC<br>AS7C31024-15TPC | AS7C1024-20TPC<br>AS7C31024-20TPC |
| Plastic DIP, 400 mil | | AS7C1024-12PC<br>AS7C31024-12PC | AS7C1024-15PC<br>AS7C31024-15PC | AS7C1024-20PC<br>AS7C31024-20PC |
| Plastic SOJ, 300 mil | AS7C1024-10TJC | AS7C1024-12TJC<br>AS7C31024-12TJC | AS7C1024-15TJC<br>AS7C31024-15TJC<br>AS7C31024-15TJI | AS7C1024-20TJC<br>AS7C31024-20TJC<br>AS7C31024-20TJI |
| Plastic SOJ, 400 mil | AS7C1024-10JC | AS7C1024-12JC<br>AS7C31024-12JC | AS7C1024-15JC<br>AS7C1024-15JI<br>AS7C31024-15JC<br>AS7C31024-15JI | AS7C1024-20JC<br>AS7C1024-20JI<br>AS7C31024-20JC<br>AS7C31024-20JI |
| TSOP 8×20 | | AS7C1024-12TC<br>AS7C31024-12TC | AS7C1024-15TC<br>AS7C31024-15TC | AS7C1024-20TC<br>AS7C31024-20TC |

Shaded areas contain advance information.

## AS7C1024 part numbering system

| AS7C | X | | 1024 | –XX | X | | | X |
|---|---|---|---|---|---|---|---|---|
| SRAM prefix | Blank<br>3 | = 5V CMOS<br>= 3.3V CMOS | Device number | Access time | Package: | TP = PDIP 300 mil<br>TJ = SOJ 300 mil<br>T = TSOP 8×20 | P = PDIP 400 mil<br>J = SOJ 400 mil | C = Commercial temperature range, 0°C to 70 °C<br>I = Industrial temperature range, -40°C to 85°C |


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# Representatives and sales offices

## DOMESTIC REPS

### ALABAMA

Concord Component Reps
Madison, AL
(205) 772-8883

### ARIZONA

O'Donnell Associates Southwest
Phoenix, AZ
(602) 944-9542

### ARKANSAS

Southern States Marketing
Richardson, TX
(214) 238-7500

### CALIFORNIA

North:

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(graphics)
Cupertino, CA
(408) 252-3880

Centaur North Inc. (memories)
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(408) 894- 0182

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Competitive Technology
Irvine, CA
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Technology Sales
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Broomall, PA
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Palm Harbor, FL 34684
(813) 781-1706

Southern States Marketing
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Southern States Marketing
Ft. Lauderdale, FL 33309
(954) 776-4330

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### ILLINOIS

El-Mech
Chicago, IL
(773) 794-9100

CenTech
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(314) 291-4230

### INDIANA

CC Electro Sales
Indianapolis, IN
(317) 921-5000

### KANSAS

CenTech
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### KENTUCKY

CC Electro Sales
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Southern States Marketing
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Bloomfield Hills, MI
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### MISSISSIPPI

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### NEW JERSEY

ERA Associates
Commack, NY
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### NEW YORK

ERA Associates
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(516) 543-0510

Tri-Tech Electronics
Binghamton, NY
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Tri-Tech Electronics
East Rochester, NY
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### NORTH CAROLINA

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Lyndhurst, OH
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O'Donnell Associates Southwest
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### WASHINGTON

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