

5.8-17GHz Low Noise Amplifier

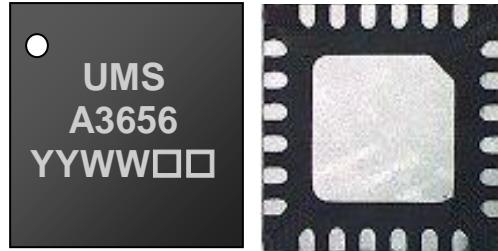
GaAs Monolithic Microwave IC in SMD leadless package

Description

The CHA3656-QAG is a two-stage self-biased wide band monolithic low noise amplifier.

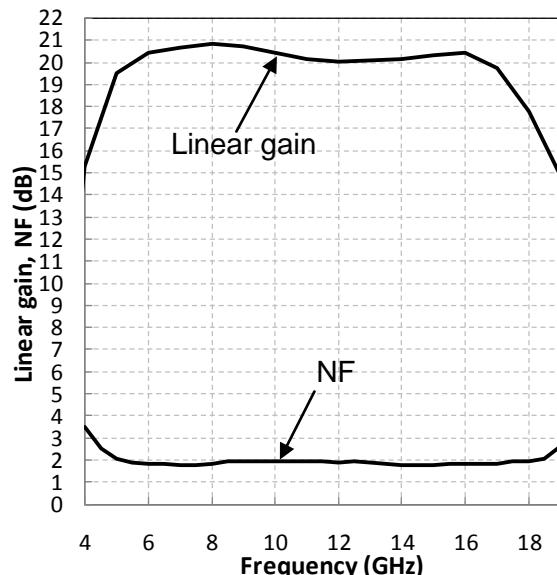
The circuit is manufactured with a pHEMT process, $0.25\mu\text{m}$ gate length, via holes through the substrate, air bridges and electron beam gate lithography.

It is supplied in RoHS compliant SMD package.



Main Features

- Broadband performances: 5.8-17GHz
- 1.9dB noise figure
- 22dBm 3rd order intercept point
- DC bias: $V_d=4\text{Volt}$ @ $I_d=55\text{mA}$
- 16L-QFN3x3
- MSL1



Main Characteristics

Tamb.= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	5.8		17	GHz
Gain	Linear Gain	18	20		dB
NF	Noise Figure		1.9	2.2	dB
OIP3	3rd order intercept point	20	22		dBM
Id	Drain current	40	55	70	dBM

Main Characteristics

Tamb.= +25°C, Vd1, 2 = +4V, P1 = N2 = +1V ⁽¹⁾

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	5.8		17	GHz
Gain	Linear Gain	18	20		dB
ΔG	Gain flatness		±0.5		dB
NF	Noise Figure		1.9	2.2	dB
R _{Llin}	Input return loss		-8	-7	dB
R _{Lout}	Output return loss		-10	-8	dB
OIP3	3rd order intercept point	+20	+22		dBm
I _d	Drain current	40	55	70	mA

These values are representative of onboard measurements as defined on the drawing in paragraph "Evaluation mother board".

⁽¹⁾ The other leads are not connected

Absolute Maximum Ratings ⁽¹⁾

Tamb.= +25°C

Symbol	Parameter	Values	Unit
V _d	Drain bias voltage	+4.5	V
P _{in}	RF input power	+10	dBm
T _j	Junction temperature ⁽²⁾	175	°C
T _a	Operating temperature range	-40 to +85	°C
T _{stg}	Storage temperature range	-55 to +150	°C

⁽¹⁾ Operation of this device above anyone of these parameters may cause permanent damage.

Typical Bias Conditions

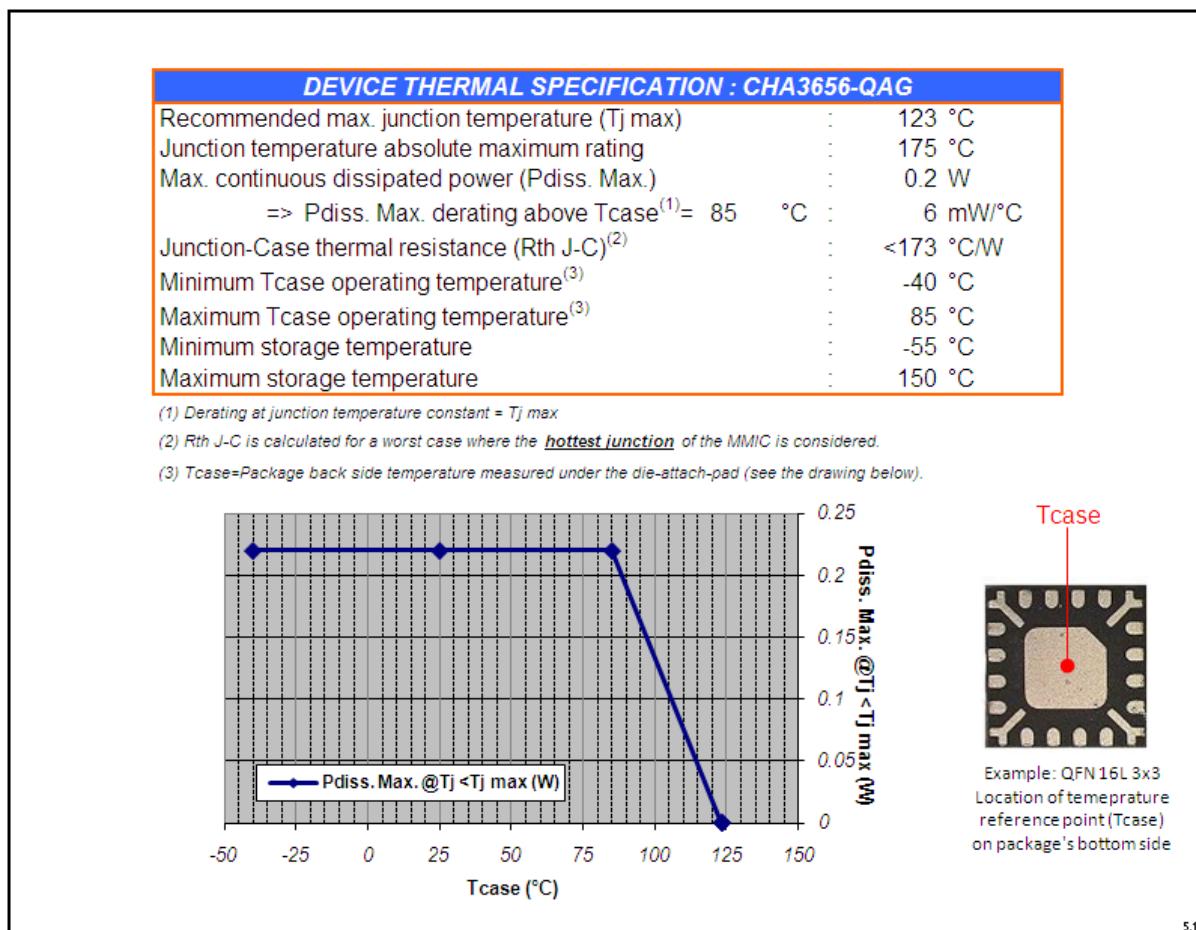
Tamb.= +25°C

Symbol	Pad N°	Parameter	Values	Unit
V _{d1}	16	DC drain voltage	+4.0	V
V _{d2}	14	DC drain voltage	+4.0	V
P ₁	5	DC gate voltage	+1.0	V
N ₂	8	DC gate voltage	+1.0	V

Device thermal performances

All the figures given in this section are obtained assuming that the QFN device is cooled down only by conduction through the package thermal pad (no convection mode considered). The temperature is monitored at the package back-side interface (T_{case}) as shown below. The system maximum temperature must be adjusted in order to guarantee that T_{case} remains below than the maximum value specified in the next table. So, the system PCB must be designed to comply with this requirement.

A derating must be applied on the dissipated power if the T_{case} temperature can not be maintained below than the maximum temperature specified (see the curve $P_{diss. Max.}$) in order to guarantee the nominal device life time (MTTF).



Typical Package Sij parameters

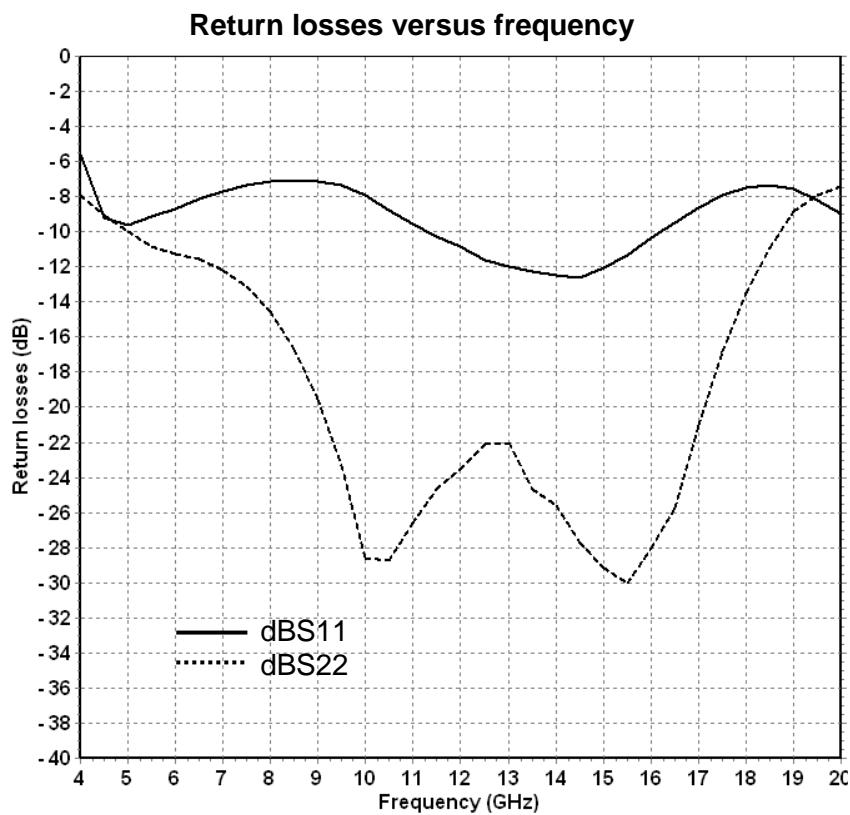
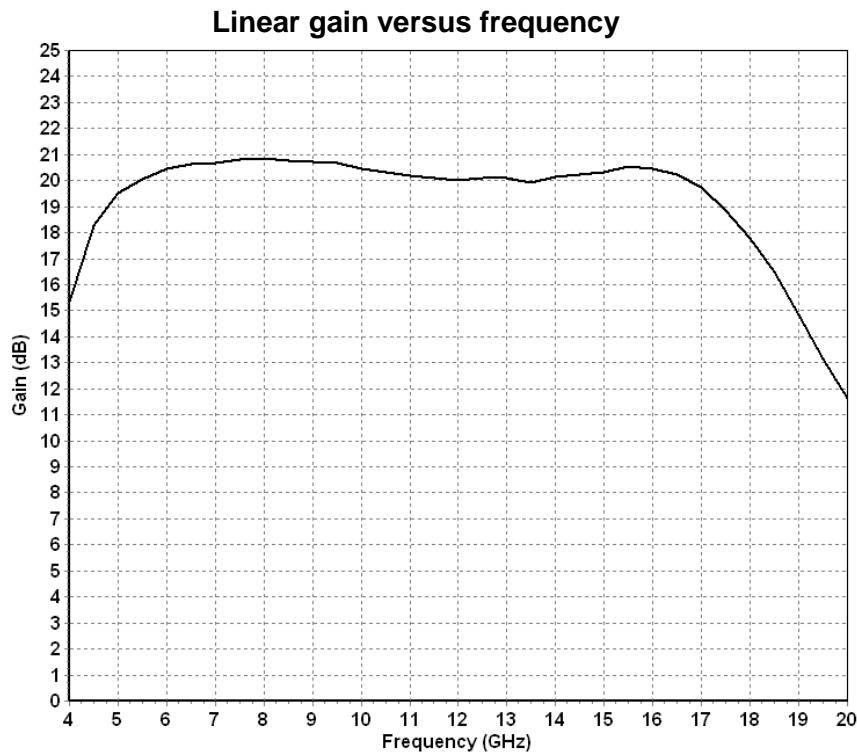
Tamb.= +25°C, Vd1, 2 = +4.0V, P1, N2 = +1V, Id = 55mA

Freq (GHz)	S11 (dB)	PhS11 (°)	S12 (dB)	PhS12 (°)	S21 (dB)	PhS21 (°)	S22 (dB)	PhS22 (°)
2.0	-0.3	-78.5	-27.9	-15.6	-67.8	-175.2	-0.5	-76.5
3.0	-1.1	-134.5	1.1	-98.1	-64.0	81.3	-3.5	-122.3
4.0	-5.6	121.8	15.3	143.7	-52.3	-142.7	-7.9	-142.7
5.0	-9.6	-25.2	19.5	36.9	-43.6	128.4	-10.0	-157.6
6.0	-8.7	-82.9	20.5	-39.7	-40.1	72.6	-11.3	-173.0
7.0	-7.7	-115.1	20.7	-101.6	-38.1	25.9	-12.2	160.9
8.0	-7.1	-143.8	20.9	-155.3	-37.4	-16.1	-14.6	125.4
9.0	-7.1	-175.5	20.7	154.5	-36.5	-49.8	-19.5	89.3
10.0	-7.9	154.1	20.5	107.8	-35.8	-84.8	-28.6	21.5
11.0	-9.6	125.1	20.2	64.5	-34.9	-121.2	-26.6	-86.7
12.0	-10.9	98.7	20.0	22.9	-35.0	-158.4	-23.5	-131.3
13.0	-12.0	73.3	20.1	-19.0	-35.1	169.1	-22.1	-172.0
14.0	-12.5	40.5	20.1	-60.0	-35.3	131.9	-25.6	171.4
15.0	-12.0	0.5	20.3	-103.4	-35.7	95.8	-29.2	165.1
16.0	-10.4	-55.1	20.5	-151.7	-37.4	56.1	-28.0	152.3
17.0	-8.6	-110.8	19.7	156.8	-43.0	20.5	-21.1	56.7
18.0	-7.5	-164.0	17.8	105.6	-50.7	44.6	-13.5	-14.1
19.0	-7.6	147.2	14.9	58.3	-42.5	62.1	-8.9	-60.7
20.0	-9.0	100.6	11.6	20.1	-39.6	30.0	-7.4	-95.3
21.0	-10.4	50.1	8.7	-15.7	-38.5	-1.5	-5.8	-118.7
22.0	-10.8	-6.9	5.9	-48.6	-38.7	-54.3	-4.9	-142.0
23.0	-9.6	-57.4	3.3	-75.4	-42.4	-95.2	-4.7	-164.6
24.0	-7.4	-99.0	1.4	-107.8	-44.0	-100.4	-4.4	179.5
25.0	-5.9	-131.4	-0.9	-135.3	-41.4	-145.0	-4.0	159.8
26.0	-4.9	-159.6	-2.2	-161.6	-37.9	171.2	-3.9	137.7
27.0	-4.6	171.9	-2.5	167.8	-35.1	122.7	-4.0	116.8
28.0	-6.0	141.8	-1.7	122.3	-31.4	70.6	-4.4	97.3
29.0	-9.2	150.8	-3.7	46.2	-30.6	13.8	-4.1	76.6
30.0	-5.5	134.5	-12.2	-8.7	-33.6	-34.0	-4.6	53.7
31.0	-5.1	105.8	-20.4	-39.7	-35.2	-72.8	-4.7	32.6
32.0	-5.8	80.7	-30.6	-46.3	-41.0	-170.8	-5.4	15.0
33.0	-5.9	47.6	-30.5	-19.5	-40.3	53.0	-5.4	-5.4
34.0	-10.3	-20.6	-24.9	-95.0	-29.7	-57.6	-5.1	-16.1
35.0	-8.0	116.3	-29.5	142.3	-36.2	177.4	-3.8	-46.6
36.0	-4.0	46.7	-33.3	51.3	-40.2	54.7	-4.1	-79.3
37.0	-3.0	1.3	-36.2	-3.6	-38.4	-20.4	-4.8	-113.6
38.0	-2.9	-40.9	-40.9	7.0	-40.9	-54.1	-5.3	-147.5
39.0	-3.8	-84.5	-34.9	7.9	-41.0	-54.1	-5.5	179.8
40.0	-4.7	-124.0	-34.8	-26.1	-40.5	-84.5	-5.7	153.9

Typical Board Measurements

Tamb.= +25°C, Vd1, 2 = +4.0V, P1, N2 = +1V, Id = 55mA

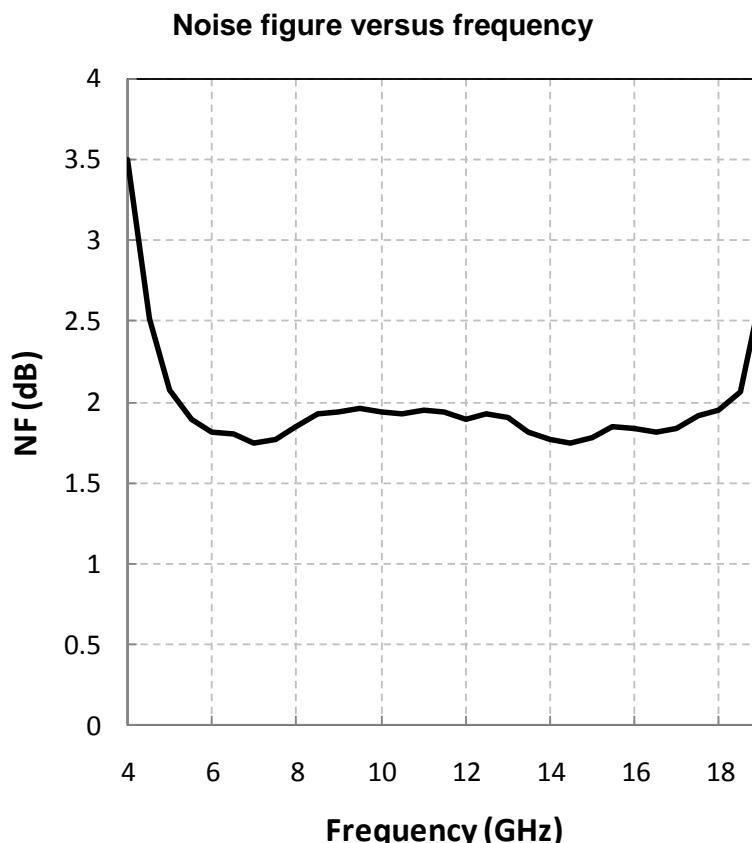
Losses due to board are de-embedded. Measurements are given in the [QFN access plan](#).



Typical Board Measurements

Tamb.= +25°C, Vd1, 2 = +4.0V, P1, N2 = +1V, Id = 55mA

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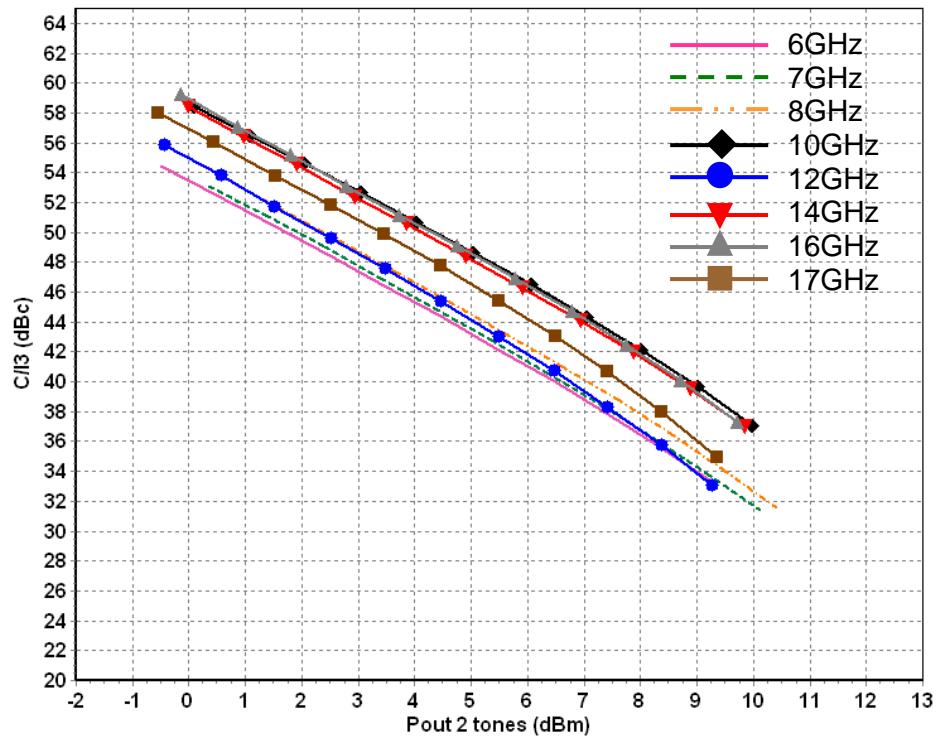


Typical Board Measurements

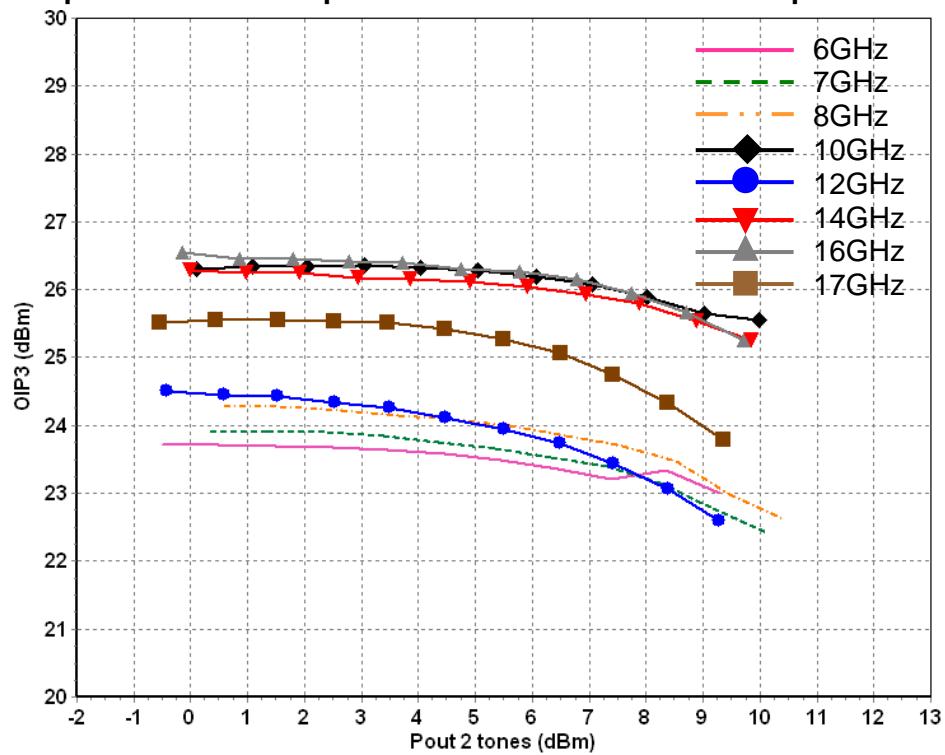
Tamb.= +25°C, Vd1, 2 = +4.0V, P1, N2 = +1V, Id = 55mA

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C/I3 versus Output Power 2 tones at ambient temperature



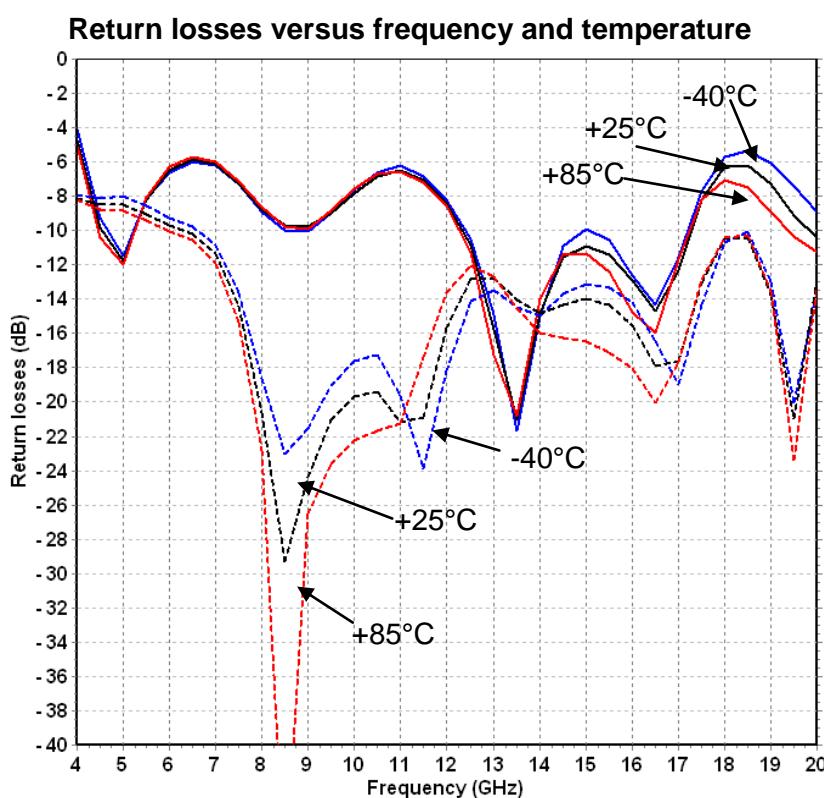
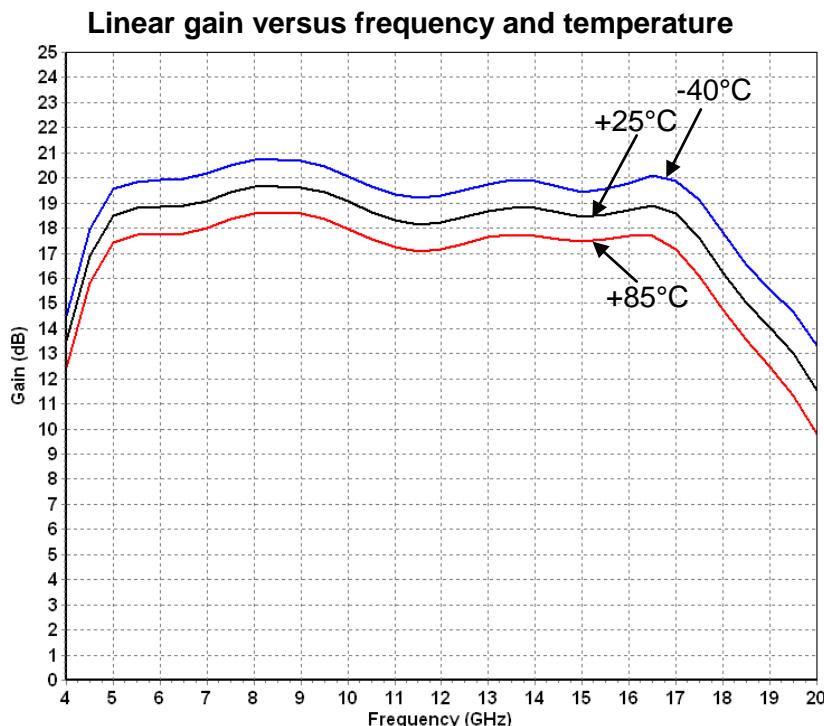
Output IP3 versus Output Power 2 tones at ambient temperature



Typical Board Measurements

Vd1, 2 = +4.0V, P1, N2 = +1V, Id = 55mA

Losses due to board are not de-embedded. Measurements are given in the [connectors' access plan](#).

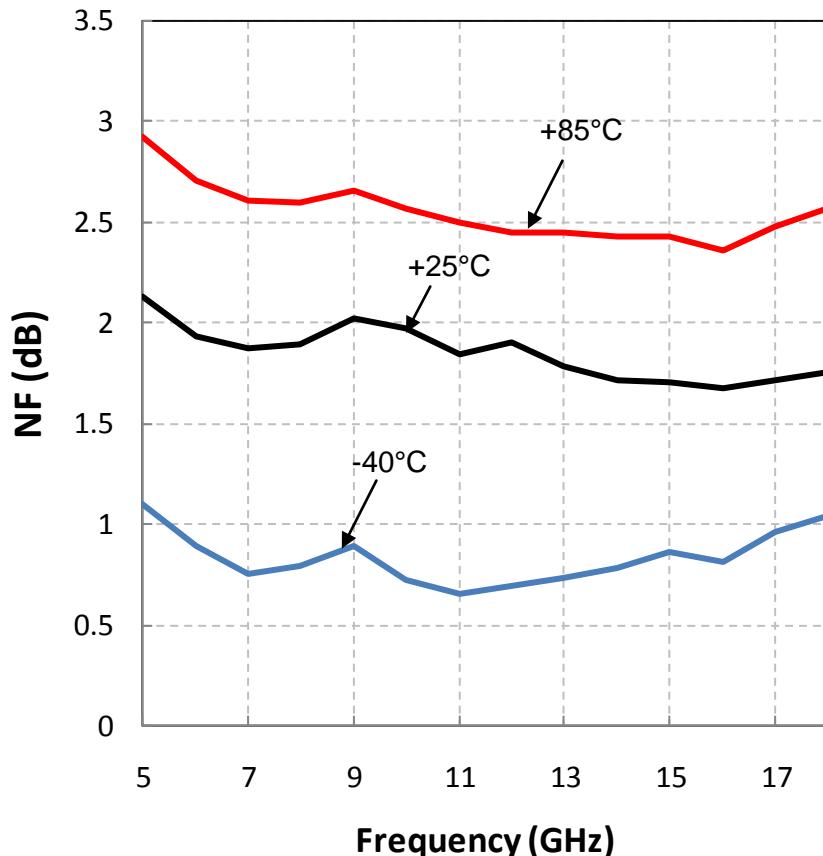


Typical Board Measurements

Vd1, 2 = +4.0V, P1, N2 = +1V, Id = 55mA

Losses due to board are de-embedded. Measurements are given in the [QFN access plan](#).

Noise figure versus frequency and temperature

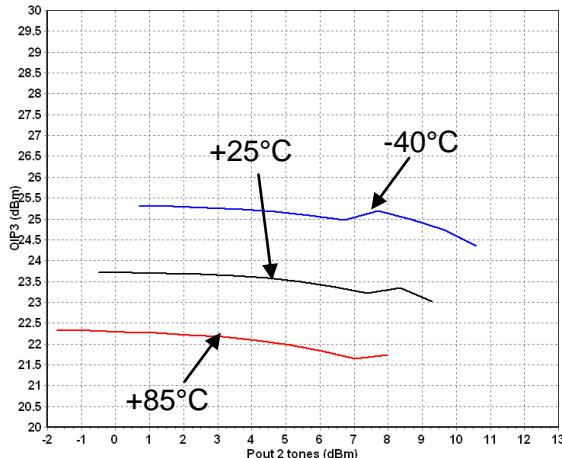


Typical Board Measurements

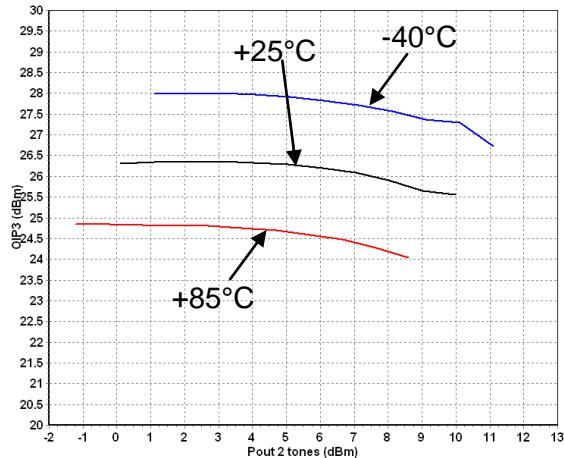
Vd1, 2 = +4.0V, P1, N2 = +1V, Id = 55mA

Losses due to board are de-embedded. Measurements are given in the [QFN access plan](#).

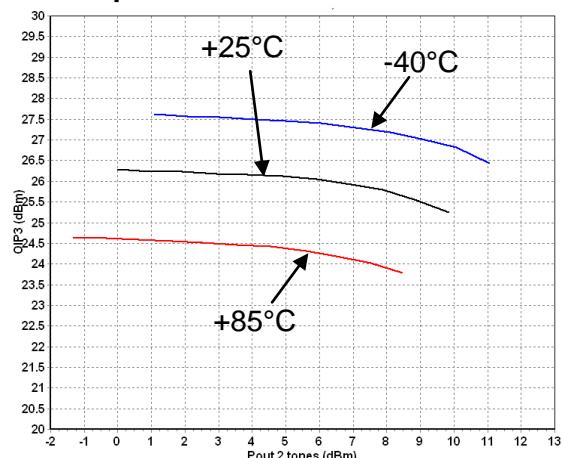
Output IP3 versus Temperature and Output Power 2 tones at 6GHz



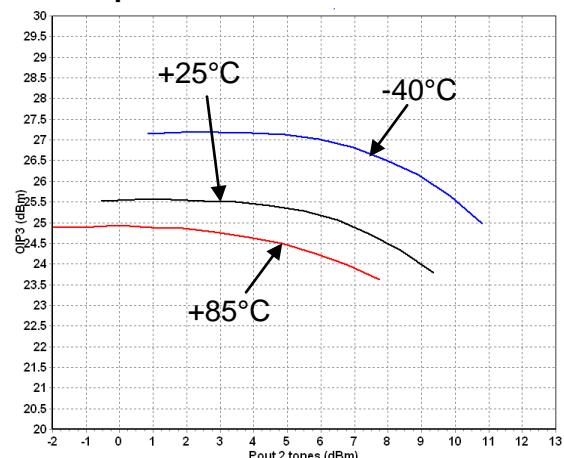
Output IP3 versus Temperature and Output Power 2 tones at 10GHz

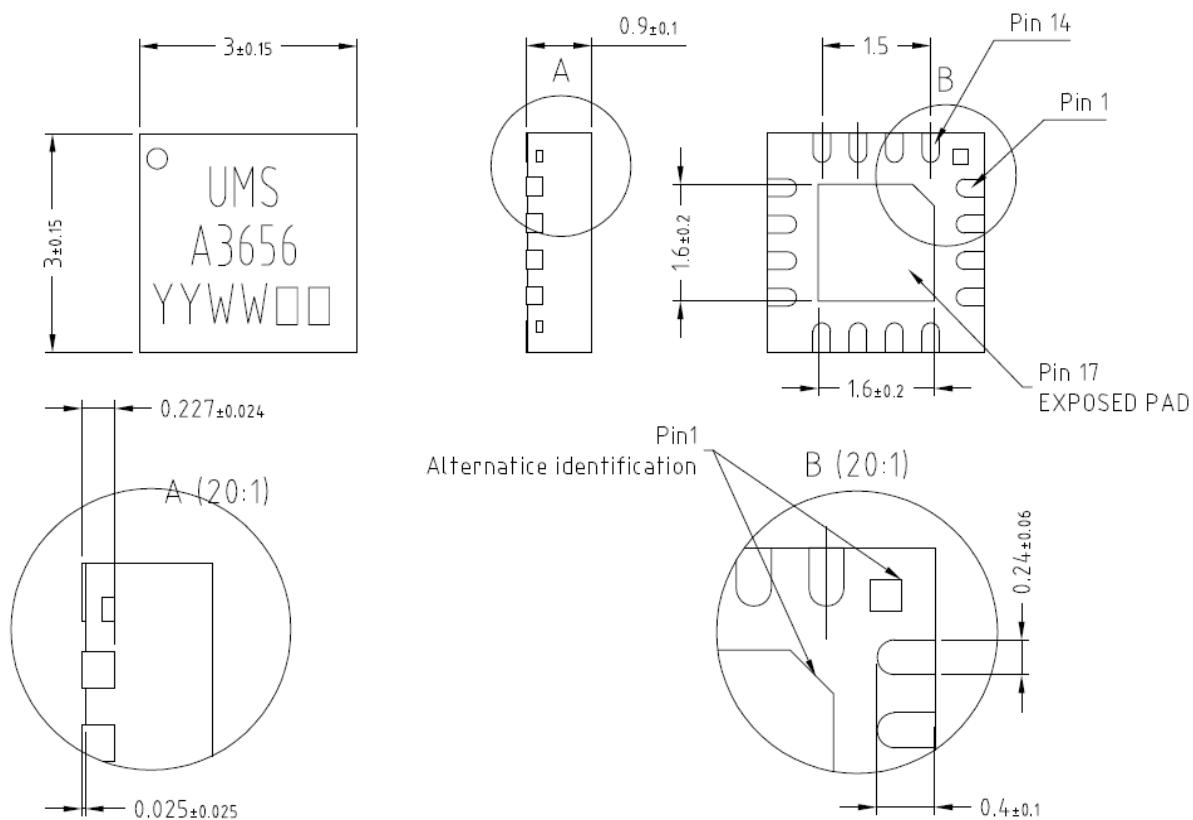


Output IP3 versus Temperature and Output Power 2 tones at 14GHz



Output IP3 versus Temperature and Output Power 2 tones at 17GHz



Package outline ⁽¹⁾

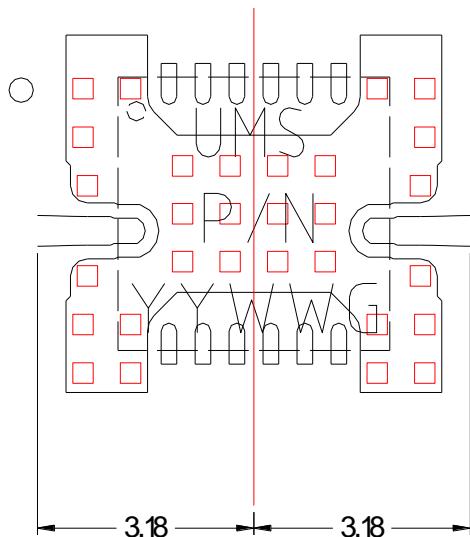
Matt tin, Lead Free	(Green)	1-	Nc	11-	Gnd ⁽²⁾
Units :	mm	2-	Gnd ⁽²⁾	12-	Nc
From the standard :	JEDEC MO-220 (VGGD)	3-	RF in	13-	Nc
		4-	Gnd ⁽²⁾	14-	VD2
25-	GND	5-	P1	15-	Gnd ⁽²⁾
		6-	NC	16-	VD1
		7-	P2		
		8-	N2		
		9-	Gnd ⁽²⁾		
		10-	RF out		

⁽¹⁾ The package outline drawing included to this data-sheet is given for indication. Refer to the application note AN0017 (<http://www.ums-gaas.com>) for exact package dimensions.

⁽²⁾ It is strongly recommended to ground all pins marked "Gnd" through the PCB board. Ensure that the PCB board is designed to provide the best possible ground to the package.

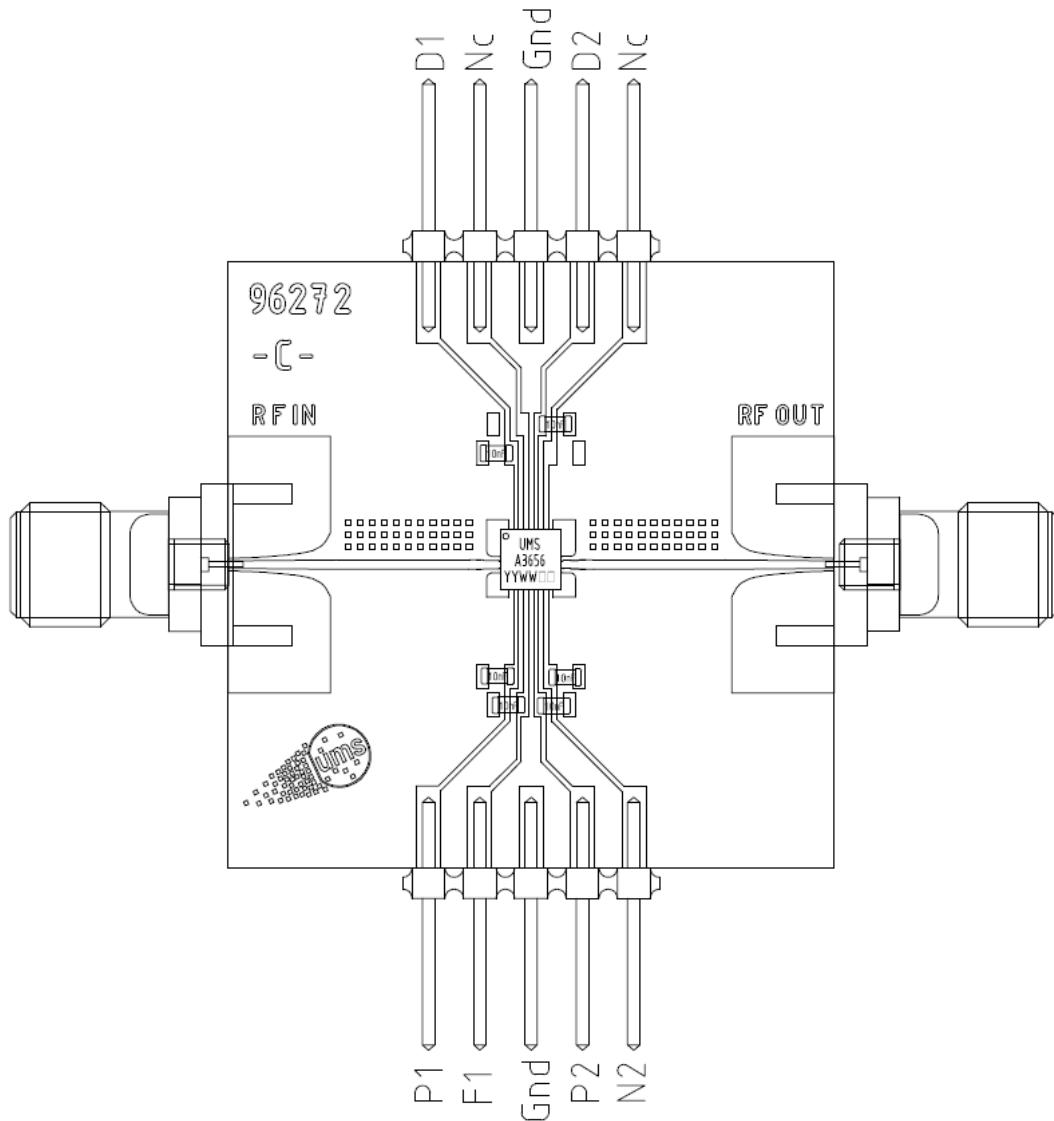
Definition of the Sij reference planes

The reference planes used for Sij measurements given above are symmetrical from the symmetrical axis of the package (see drawing beside). The input and output reference planes are located at 3.18mm offset (input wise and output wise respectively) from this axis. Then, the given Sij parameters incorporate the land pattern of the evaluation motherboard recommended in paragraph "Evaluation mother board".



Evaluation mother board

- Compatible with the proposed footprint.
- Based on typically Ro4003 / 8mils or equivalent.
- Using a micro-strip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.
- Decoupling capacitors of $10\text{nF} \pm 10\%$ are recommended for all DC accesses.
- See application note AN0017 for details.



Recommended package footprint

Refer to the application note AN0017 available at <http://www.ums-gaas.com> for package footprint recommendations.

SMD mounting procedure

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017.

Recommended environmental management

Refer to the application note AN0019 available at <http://www.ums-gaas.com> for environmental data on UMS package products.

Recommended ESD management

Refer to the application note AN0020 available at <http://www.ums-gaas.com> for ESD sensitivity and handling recommendations for the UMS package products.

Ordering Information

QFN 3x3 RoHS compliant package:	CHA3656-QAG/XY	
	Stick: XY = 20	Tape & reel: XY = 21

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