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FPD3000SOT89CE

LOW-NOISE HIGH-LINEARITY PACKAGED pHEMT

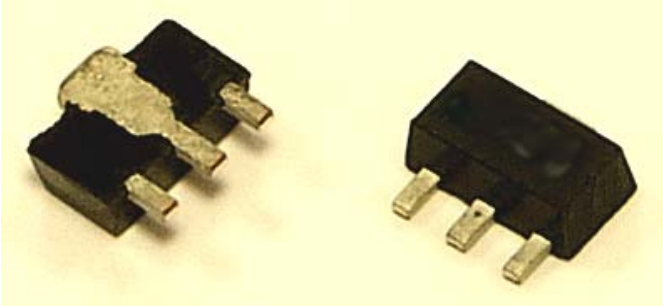
Package: SOT89

Product Description

The FPD3000SOT89CE is a packaged depletion mode AlGaAs/InGaAs pseudomorphic High Electron Mobility Transistor (pHEMT). It features a 0.25µmx1500µm Schottky barrier gate, defined by high-resolution stepper-based photolithography. The double recessed gate structure minimizes parasitics to optimize performance. The epitaxial structure is designed for improved linearity over a range of bias conditions and input power levels.

Optimum Technology Matching® Applied

- ☐ GaAs HBT
- ☐ GaAs MESFET
- ☐ InGaP HBT
- ☐ SiGe BiCMOS
- ☐ Si BiCMOS
- ☐ SiGe HBT
- ☑ GaAs pHEMT
- ☐ Si CMOS
- ☐ Si BJT
- ☐ GaN HEMT
- ☐ InP HBT
- ☐ RF MEMS
- ☐ LDMOS



Features

- 30dBm Output Power (P1dB)
- 13dB Small-Signal Gain (SSG)
- 1.3dB Noise Figure
- 45dBm O_{IP3}
- 45% Power-Added Efficiency
- FPD3000SOT89CE: RoHS Compliant (Directive 2002/95/EC)

Applications

- Drivers or Output Stages in PCS/Cellular Base Station Transmitter Amplifiers
- High Intercept-point LNAs
- WLL, WLAN, and Other Types of Wireless Infrastructure Systems

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
P_{1dB} Gain Compression	29	30		dBm	V_{DS}=5V, I_{DS}=50% I_{DSS}
Small-Signal Gain (SSG)	11.5	13		dB	V_{DS}=5V, I_{DS}=50% I_{DSS}
PAE		45		%	V_{DS}=5V, I_{DS}=50% I_{DSS}, P_{OUT}=P_{1dB}
Noise Figure (NF)		1.3		dB	V_{DS}=5V, I_{DS}=50% I_{DSS}; V_{DS}=5V, I_{DS}=25% I_{DSS}
		0.9		dB	V_{DS}=5V, I_{DS}=25% I_{DSS}. Matched for optimal power.
OIP_3 (15dB to 5dB below P_{1dB})		42		dBm	Matched for best IP_3
		45		mA	V_{DS}=1.3V, V_{GS}=0V
Saturated Drain-Source Current (I_{DSS})	750	930	1100	mA	V_{DS}=1.3V, V_{GS}=0V
Maximum Drain-Source Current (I_{MAX})		1.5		mA	V_{DS}=1.3V, V_{GS}≅+1V
Transconductance (GM)		800		ms	V_{DS}=1.3V, V_{GS}=0V
Gate-Source Leakage Current (IGSO)		2	20	µA	V_{GS}=-5V
Pinch-Off Voltage (V_P)	|0.7|	|1.0	|1.3|	V	V_{DS}=1.3V, I_{DS}=3mA
Gate-Source Breakdown Voltage (V_{BDGS})	|12|	|16|		V	I_{GS}=3mA
Gate-Drain Breakdown Voltage (V_{BDGD})	|12|	|16|		V	I_{DS}=3mA
Thermal Resistivity (θJC) *		35		°C/W	

*Note: $T_{AMBIENT}$=22 °C, RF specifications measured at f=1850GHz using CW signal (except as noted).

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Absolute Maximum Ratings[1]

Parameter	Rating	Unit
Drain-Source Voltage (V_{DS}) ($-3V<V_{GS}<-0.5V$)	8	V
Gate-Source Voltage (V_{GS}) ($0V<V_{DS}<+8V$)	-3	V
Drain-Source Current (I_{DS}) (For $V_{DS}<2V$)	I_{DSS}	
Gate Current (I_G) (Forward or reverse)	30	mA
RF Input Power (P_{IN})[2] (Under any acceptable bias state)	600	mW
Channel Operating Temperature (T_{CH}) (Under any acceptable bias state)	175	°C
Storage Temperature (T_{STG}) (Non-Operating Storage)	-40 to 150	°C
Total Power Dissipation (P_{TOT})[3, 4, 5]	3.5	W
Gain Compression (Under bias conditions)	5	dB
Simultaneous Combination of Limits[6] (2 or more max. limits)		

Notes:
[1] $T_{AMBIENT}=22°C$ unless otherwise noted; exceeding any one of these absolute maximum ratings may cause permanent damage to the device.
[2] Max. RF input limit must be further limited if input VSWR>2.5:1.
[3] Users should avoid exceeding 80% of 2 or more Limits simultaneously.
[4] Total Power Dissipation (P_{TOT}) defined as $(P_{DC}+P_{IN})-P_{OUT}$, where P_{DC}: DC Bias Power, P_{IN}: RF Input Power, P_{OUT}: RF Output Power.
Total Power Dissipation to be de-rated as follows above 22 °C:
$P_{TOT}=3.5-(0.028W/°C)xT_{PACK}$, where T_{PACK}=source tab lead temperature above 22 °C. (Coefficient of de-rating formula is Thermal Conductivity.)
Exampe: For a 65°C carrier temperature: $P_{TOT}=3.5W-(0.028x(65-22))=2.3W$

Caution! ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

RoHS status based on EUDirective2002/95/EC (at time of this document revision).

Biasing Guidelines

Active bias circuits provide good performance stabilization over variations of operating temperature, but require a larger number of components compared to self-bias or dual-biased. Such circuits should include provisions to ensure that gate bias is applied before drain bias.

Dual-bias circuits are relatively simple to implement, but will require a regulated negative voltage supply for depletion-mode devices.

For standard Class A operation, an operating point of 50% of I_{DSS} is recommended. A small amount of RF gain expansion prior to the onset of compression is normal for this operating point. A class A/B Bias of 25% to 33% of I_{DSS} to achieve better OIP_3 and Noise Figure performance is suggested.

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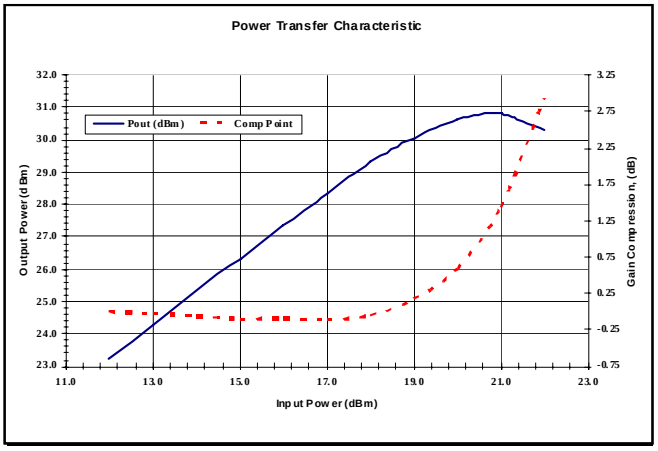
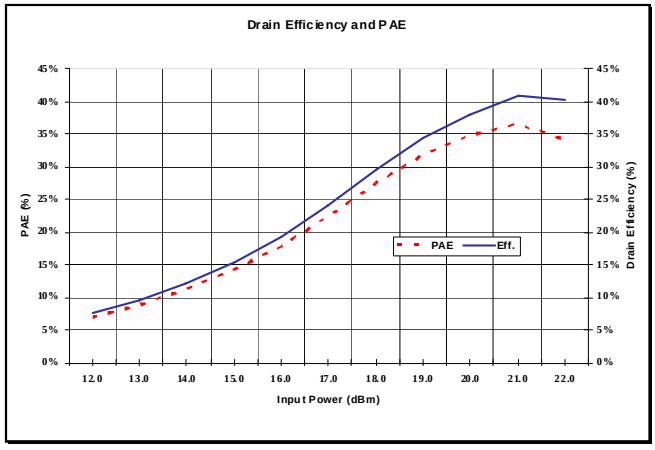
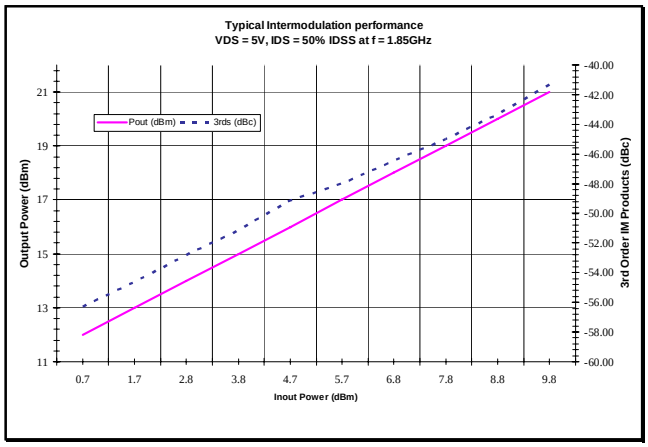
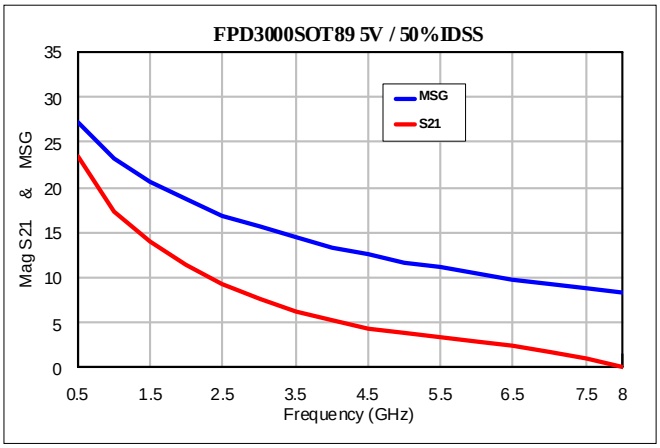
Typical Tuned RF Performance





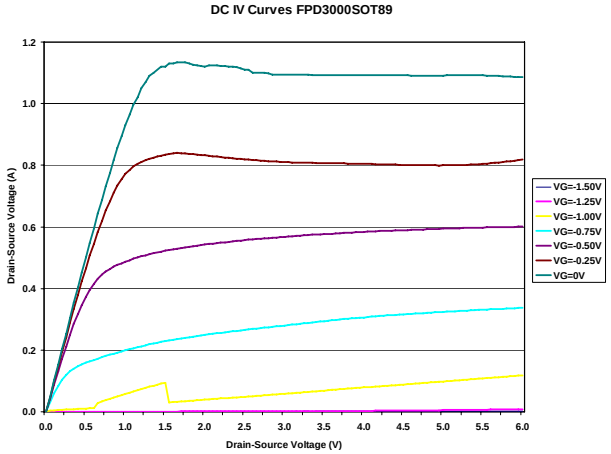
Note: Typical power and efficiency is shown above. The devices were biased nominally at V_{DS}=5V, I_{DS}=50% of I_{DSS}, at a test frequency of 1.85GHz. They were tuned (input and output tuning) for maximum output power at 1dB gain compression.





Note: pHEMT devices have enhanced intermodulation performance. This yields OIP3 values of about P_{1dB}+14dB. This IMD enhancement is affected by the quiescent bias and the matching applied to the device.

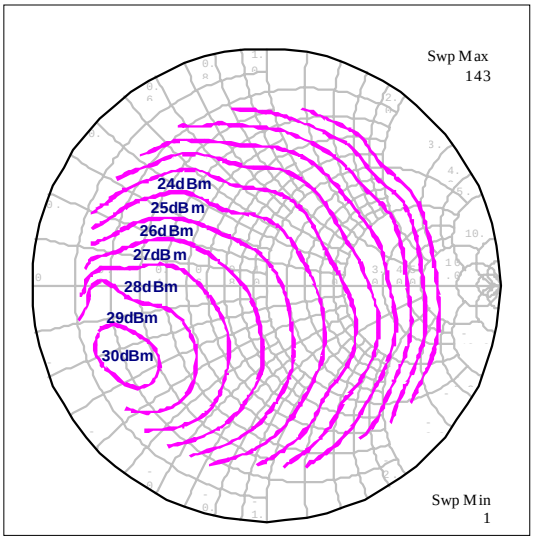
Typical I-V Characteristics



Note: The recommended method for measuring I_{DSS}, or any particular I_{DS}, is to set the Drain-Source voltage (V_{DS}) to 1.3V. This measurement point avoids the onset of spurious self-oscillation which would normally distort the current measurement (this effect has been filtered from the I-V curves presented here). Setting the V_{DS}>1.3V will generally cause errors in the current measurements, even in stabilized circuits.

Typical Output Plane Power Contours

(V_{DS}=5V, I_{DS}=50% I_{DSS})

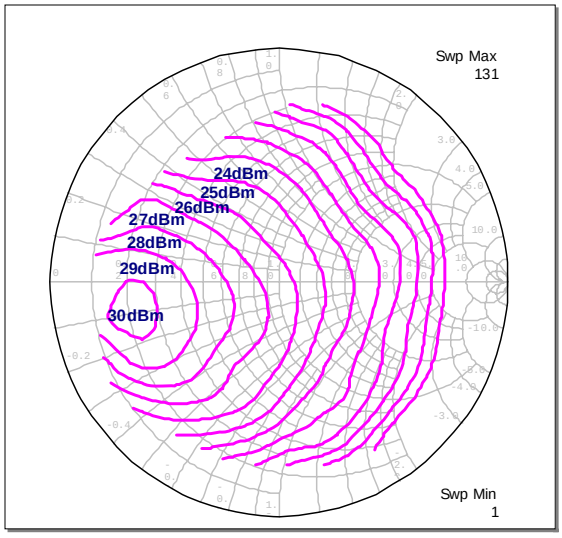


1850 MHz

Contours swept with a constant input power, set so that optimum P1dB is achieved at the point of output match.

Input (Source plane) ?s:
0.70 ? -165.5°
0.17 - j0.12 (normalized)
8.5 – j6.0 Ω

Nominal IP3 performance is obtained with this input plane match, and the output plane match as shown.



900 MHz

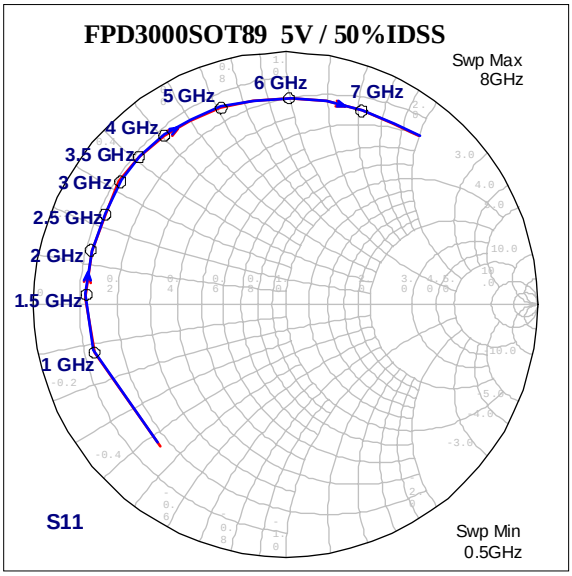
Contours swept with a constant input power, set so that optimum P1dB is achieved at the point of output match.

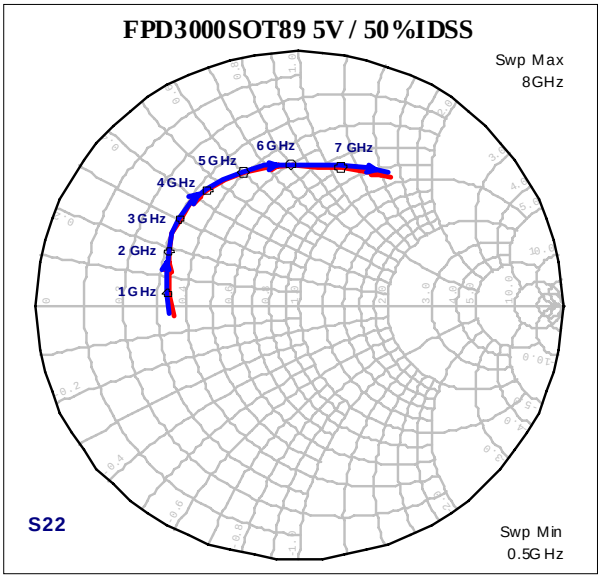
Input (Source plane) ?s:
0.78 ? -147.4°
0.13 - j0.29 (normalized)
6.5 – j14.5 Ω

Nominal IP3 performance is obtained with this input plane match, and the output plane match as shown.

Typical Scattering Parameters

(50Ω System)





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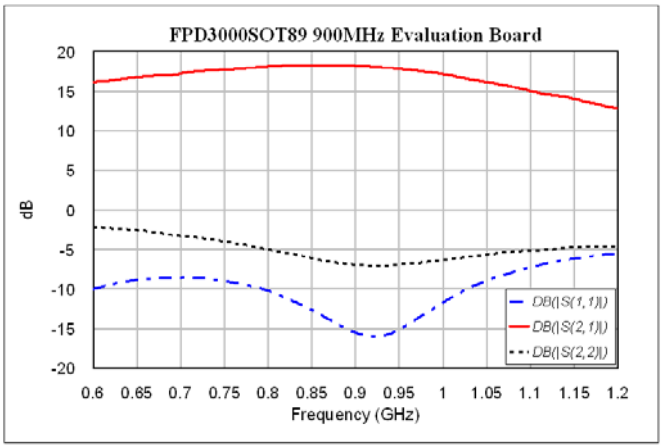
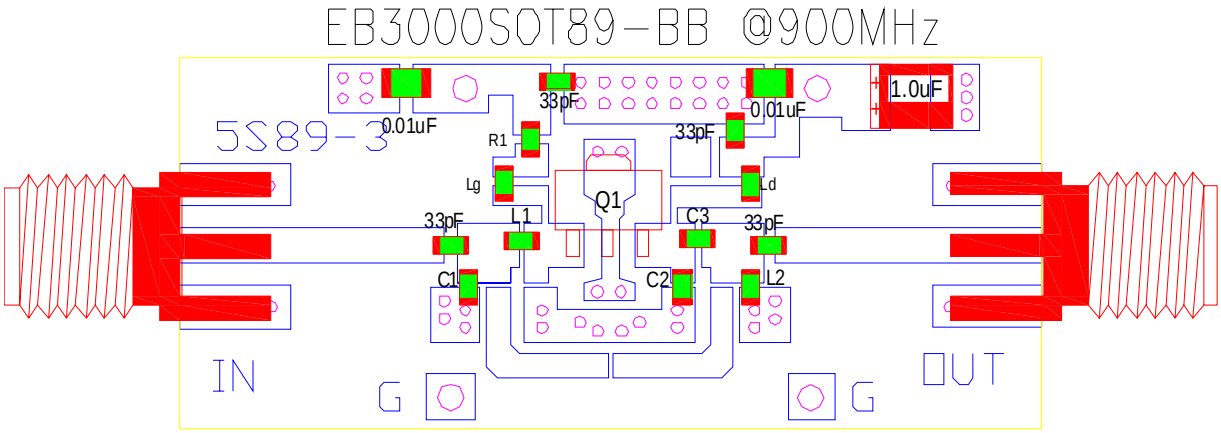
Reference Design (900MHz)

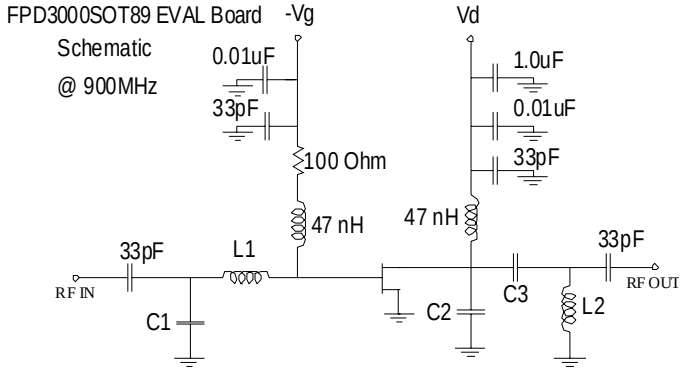


Parameter	Typ.	Unit
Frequency	900	MHz
Gain	18	dBm
P_{1dB}	30	dBm
OIP_3	41	dB
NF	1.2	dB
S11	-15	dB
S22	-7	dB
V_D	5	V
V_G	-0.4 to -0.6	V
I_D	400	mA

Note: OIP_3 measured at P_{OUT} of 19dBm per tone.

Board Layout

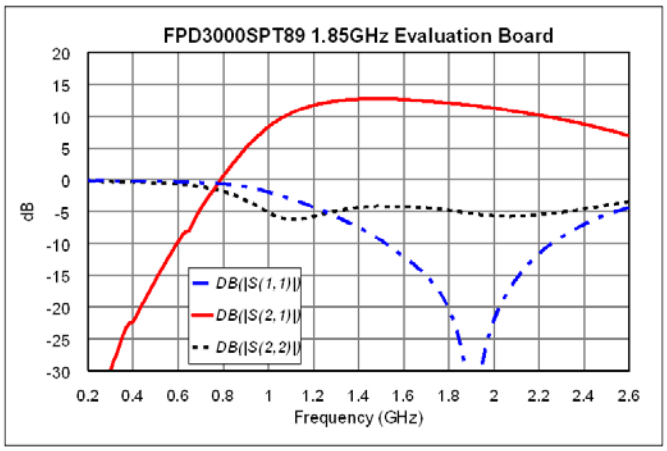




Component	Value	Description
Lg	47nH	LL1608 Toko chip
Ld	47nH	LL1608 Toko chip
L1	5.6nH	LL1605 Toko chip
L2	4.7nH	LL1605 Toko chip
C1	3.9pF	ATC 600S chip capacitor
C2	7.5pF	ATC 600S chip capacitor
C3	6.8pF	ATC 600S chip capacitor
R1	100Ω	0603 Vishay chip resistor

Eval board material is 31mil thick FR4 with 1/2oz Cu on both sides.

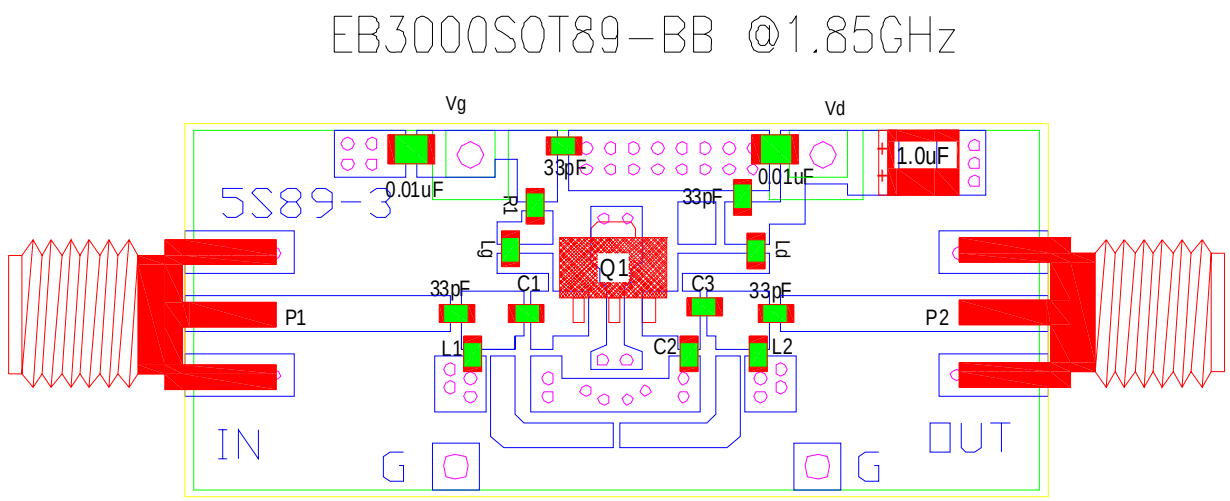
Reference Design (1.85GHz)

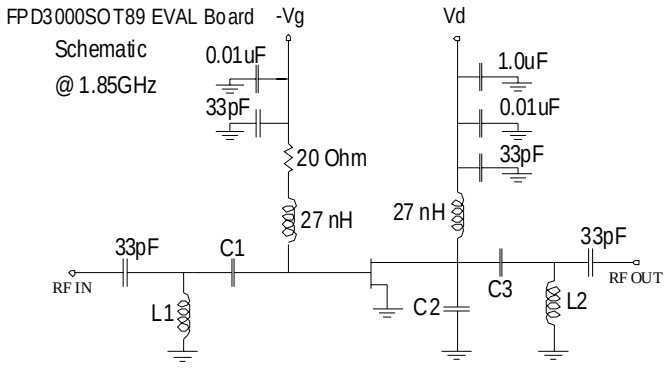


Parameter	Typ.	Unit
Frequency	1.85	GHz
Gain	12	dBm
P_{1dB}	31	dBm
OIP_3	43	dB
NF	0.9	dB
S11	-25	dB
S22	-5	dB
V_D	5	V
V_G	-0.4 to -0.6	V
I_D	400	mA

Note: OIP_3 measured at P_{OUT} of 19dBm per tone.

Board Layout





Component	Value	Description
Lg	27nH	LL1608 Toko chip
Ld	27nH	LL1608 Toko chip
L1	2.2nH	LL1605 Toko chip
L2	4.7nH	LL1605 Toko chip
C1	2.4pF	ATC 600S chip capacitor
C2	2.0pF	ATC 600S chip capacitor
C3	1.8pF	ATC 600S chip capacitor
R1	20Ω	0603 Vishay chip resistor

Eval board material is 31mil thick FR4 with 1/2oz Cu on both sides.

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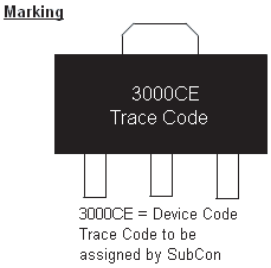
S-Parameters

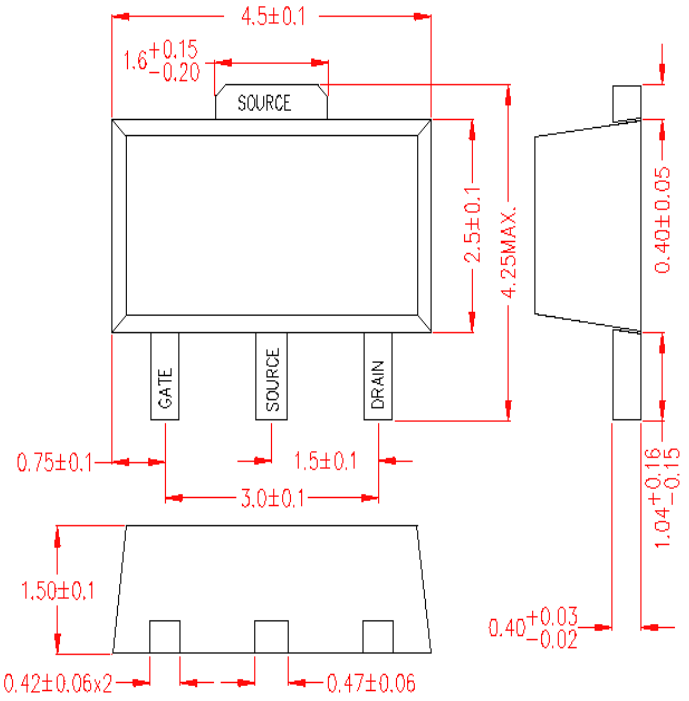
(Biased @ 5V, 50% I_{DSS})

FREQ[GHz]	S11m	S11a	S21m	S21a	S12m	S12a	S22m	S22a
0.050	0.946	-24.3	36.120	159.0	0.006	79.8	0.175	-145.5
0.300	0.824	-97.5	19.282	120.3	0.027	56.8	0.384	-150.1
0.550	0.761	-132.1	12.243	103.2	0.037	45.6	0.478	-165.4
0.800	0.779	-150.7	8.992	91.8	0.043	40.5	0.507	-172.3
1.050	0.771	-163.6	7.020	84.0	0.048	38.3	0.522	-179.1
1.300	0.775	-173.0	5.802	76.3	0.054	35.9	0.529	176.4
1.550	0.779	178.6	4.934	70.1	0.059	34.7	0.528	171.9
1.800	0.775	171.1	4.306	63.6	0.064	31.7	0.532	167.4
2.050	0.778	164.5	3.834	57.8	0.069	29.8	0.529	163.2
2.300	0.780	158.1	3.444	52.0	0.074	27.5	0.531	158.7
2.550	0.777	152.3	3.131	46.1	0.080	24.3	0.531	154.2
2.800	0.778	146.8	2.878	40.4	0.085	22.1	0.534	149.1
3.050	0.782	142.6	2.636	34.9	0.088	19.1	0.537	143.6
3.300	0.784	137.7	2.459	29.4	0.093	15.6	0.544	138.2
3.550	0.785	133.2	2.286	24.0	0.097	12.7	0.545	132.9
3.800	0.790	129.0	2.146	18.7	0.101	9.6	0.551	127.8
4.050	0.790	124.8	2.017	13.3	0.105	5.7	0.555	123.2
4.300	0.806	120.7	1.896	9.0	0.106	4.5	0.575	118.8
4.550	0.800	115.1	1.821	3.4	0.113	1.5	0.574	113.3
4.800	0.794	111.6	1.728	-1.4	0.117	-2.0	0.575	109.7
5.050	0.800	107.0	1.648	-6.7	0.121	-5.4	0.577	105.9
5.300	0.801	102.6	1.576	-11.5	0.123	-8.6	0.580	102.6
5.550	0.805	98.0	1.516	-16.5	0.128	-11.8	0.583	98.7
5.800	0.806	93.8	1.461	-21.4	0.132	-14.7	0.583	95.2
6.050	0.808	89.5	1.411	-26.2	0.136	-18.0	0.586	91.1
6.300	0.810	85.4	1.360	-31.2	0.139	-21.3	0.588	86.9
6.550	0.811	81.3	1.317	-36.3	0.143	-24.6	0.593	82.4
6.800	0.814	77.4	1.272	-41.2	0.146	-28.2	0.592	77.7
7.050	0.818	73.2	1.232	-46.3	0.151	-31.7	0.601	73.0
7.300	0.821	69.0	1.189	-51.3	0.153	-35.1	0.607	68.2
7.550	0.829	64.8	1.149	-56.4	0.157	-38.8	0.614	63.5
7.800	0.831	60.2	1.108	-61.4	0.159	-42.5	0.623	59.3
8.050	0.839	55.5	1.066	-66.3	0.160	-46.5	0.634	55.3

Part Identification



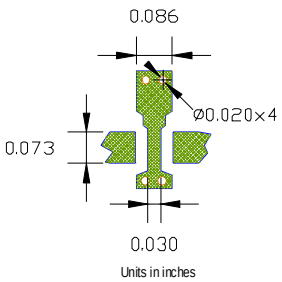
Package Outline



Tape Dimensions and Part Orientation

Tape and reel information on this part is in accordance with EIA-481-1 except where exceptions are identified

Device PCB Footprint



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Preferred Assembly Instructions

This package is compatible with both lead-free and leaded solder reflow processes as defined within IPC/JEDEC J-STD-020. The maximum package temperature should not exceed 260 °C.

Handling Precautions

To avoid damage to the devices, care should be exercised during handling. Proper Electrostatic Discharge (ESD) precautions should be observed at all stages of storage, handling, assembly, and testing.

ESD Rating

These devices should be treated as Class 0 (0V to 250V) using the human body model as defined in JEDEC Standard No. 22-A114.

MSL Rating

The device has an MSL rating of Level 2. To determine this rating, preconditioning was performed to the device per the Pb-free solder profile defined within IPC/JEDEC J-STD-020, Moisture / Reflow sensitivity classification for non-hermetic solid state surface mount devices.

Application Notes and Design Data

Application Notes and design data including S-parameters, noise paramters, and device model are available on request and from www.rfmd.com.

Reliability

A MTTF of 4.2 million hours at a channel temperature of 150 °C is achieved for the process used to manufacture this device.

Disclaimers

This product is not designed for use in any space-based or life-sustaining/supporting equipment.

Ordering Information

Description	Ordering Code
RoHS-Compliant Packaged pHEMT with enhanced passivation	FPD3000SOT89CECE
2.0 GHz Evaluation Board	EB3000SOT89-BC

Delivery Quantity	Ordering Code
Reel of 1000	FPD3000SOT89CECE
Reel of 100	FPD3000SOT89CECESR
Bag of 25	FPD3000SOT89CECESQ
Bag of 5	FPD3000SOT89CECESB

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