8-12GHz High Power Amplifier

GaAs Monolithic Microwave IC

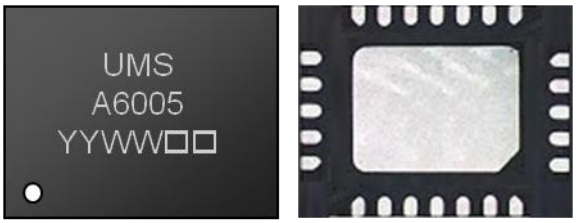
Description

The CHA6005-QEG is a high power amplifier monolithic circuit, which integrates two stages and produces 31.5dBm output power associated to a high power added efficiency of 33%.

It is designed for a wide range of applications, from professional to commercial communication systems.

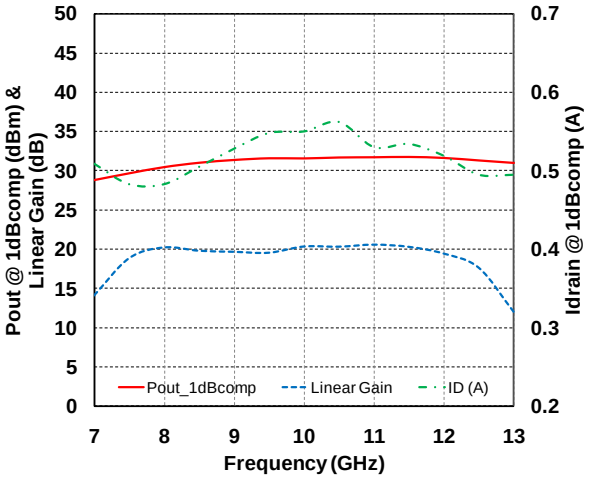
The circuit is manufactured with a pHEMT process, 0.25µm gate length, via holes through the substrate, air bridges and electron beam gate lithography.

It is supplied in a RoHS compliant SMD package.



Main Features

- High power: 31.5dBm
- High PAE: 33%
- Frequency band: 8-12GHz
- Linear gain: 20dB
- DC bias: VD=8Volt@Id=420mA
- 24L-QFN4x5
- MSL3



Main Electrical Characteristics

Tamb.= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	8		12	GHz
G	Linear Gain		20		dB
P1dB	Output Power @ 1dB comp.		31.5		dBm
PAE1dB	Power Added Efficiency @ 1dB comp.		33		%

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Electrical Characteristics

Tamb.= +25°C, VD1,2 = +8.0V

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Operating frequency	8		12	GHz
G	Small signal gain		19.5		dB
RLin	Input Return Loss		14		dB
RLout	Output Return Loss		10		dB
P1dB	Output power @ 1dBcomp		31.5		dBm
P3dB	Output power @ 3dBcomp		32		dBm
PAE1dB	Power Added Efficiency @ 1dBcomp		33		%
PAE3dB	Power Added Efficiency @ 3dBcomp		35		%
Id_1dBcomp	Supply drain current @ 1dBcomp		500		mA
Id_3dBcomp	Supply drain current @ 3dBcomp		550		mA
Idq	Supply quiescent current		420		mA
VG	Gate supply voltage		-0.7		V

These values are representative of onboard measurements and are defined in the reference plan as defined in the paragraph "Definition of reference planes ".

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Absolute Maximum Ratings (1)

Tamb.= +25°C

Symbol	Parameter	Values	Unit
VD	Drain bias voltage	9.0	V
Id	Drain bias current	700	mA
VG	Gate bias voltage	-0.25	V
Pin	Maximum peak input power overdrive	+18	dBm
Tj	Junction temperature	175	°C
Ta	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +150	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.

Typical Bias Conditions

Tamb.= +25°C

Symbol	Pad N°	Parameter	Values	Unit
VD1,2	17, 13	Drain supply voltage	8	V
VG12	18	Gate supply voltage	-0.7	V

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Device Thermal Performances

All the figures given in this section are obtained assuming that the QFN device is only cooled down by conduction through the package thermal pad (no convection mode considered).
The temperature is monitored at the package back-side interface (Tcase) as shown below.
The system maximum temperature must be adjusted in order to guarantee that Tcase remains below the maximum value specified in the next table. So, the system PCB must be designed to comply with this requirement.

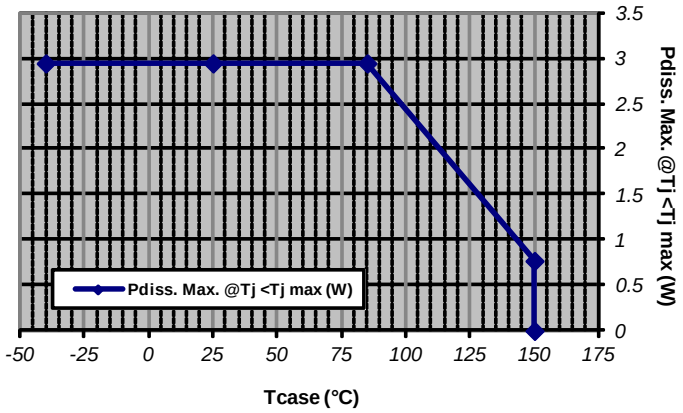
A derating must be applied on the dissipated power if the Tcase temperature cannot be maintained below the maximum temperature specified (see the curve Pdiss. Max) in order to guarantee the nominal device life time (MTTF).

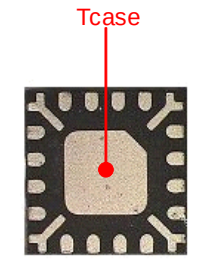
DEVICE THERMAL SPECIFICATION : CHA6005-QEG		
Recommended max. junction temperature (Tj max)	:	173 °C
Tj absolute maximum rating for 20 years minimum life time	:	175 °C
Max. continuous dissipated power (Pdiss. Max.)	:	2.9 W
=> Pdiss. Max. derating above Tcase(1)= 85 °C	:	33 mW/°C
Junction-Case thermal resistance (Rth J-C)(2)	:	<30 °C/W
Minimum Tcase operating temperature(3)	:	-40 °C
Maximum Tcase operating temperature(3)	:	85 °C
Minimum storage temperature	:	-55 °C
Maximum storage temperature	:	150 °C

(1) Derating at junction temperature constant = Tj max.

*(2) Rth J-C is calculated for a worst case considering the **hottest junction** of the MMIC and all the devices biased.*

(3) Tcase=Package back side temperature measured under the die-attach-pad (see the drawing below).





Example: QFN 16L 3x3
Location of temperature reference point (Tcase) on package's bottom side

6.4

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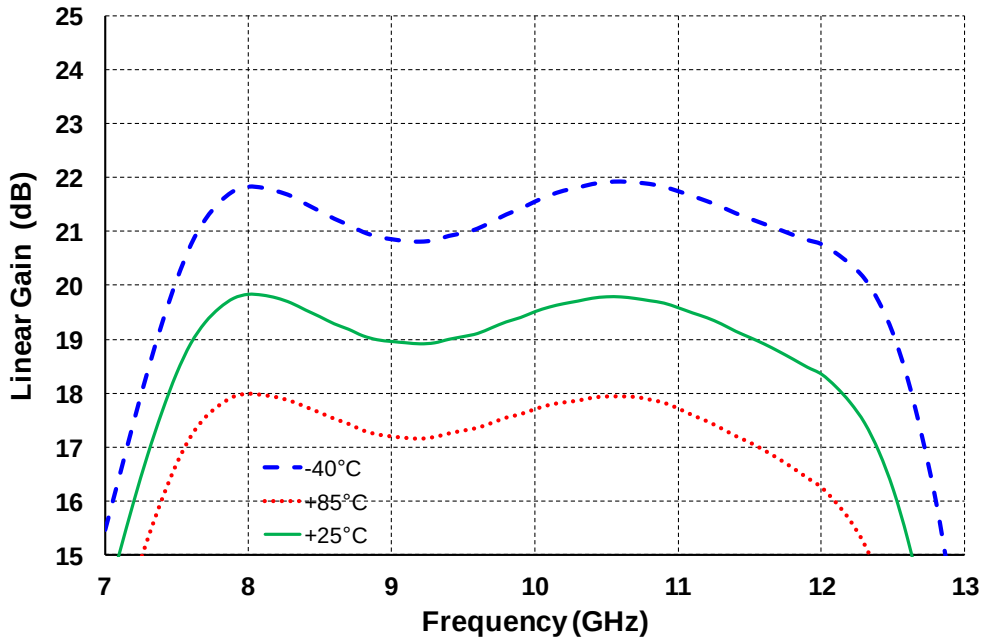
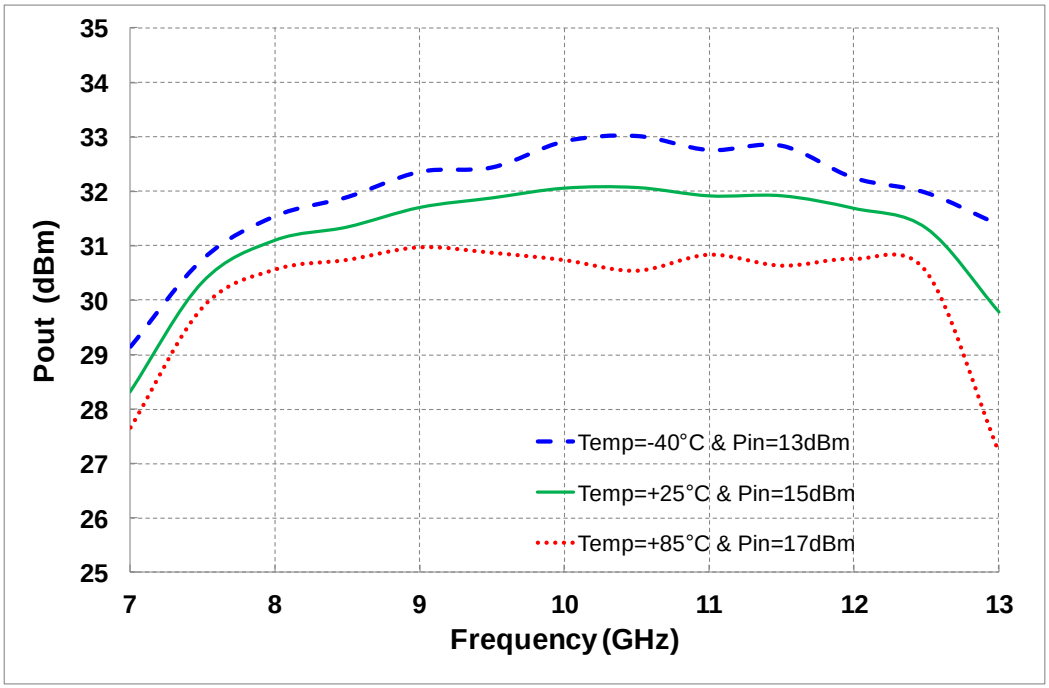
Typical Board Measurements

Temperature : -40, +25, +85°C
VD1,2 = 8V, Id (Quiescent) = 420mA, CW mode

Linear Gain versus Frequency and Temperature



Output Power at 3dBcomp versus Frequency and Temperature



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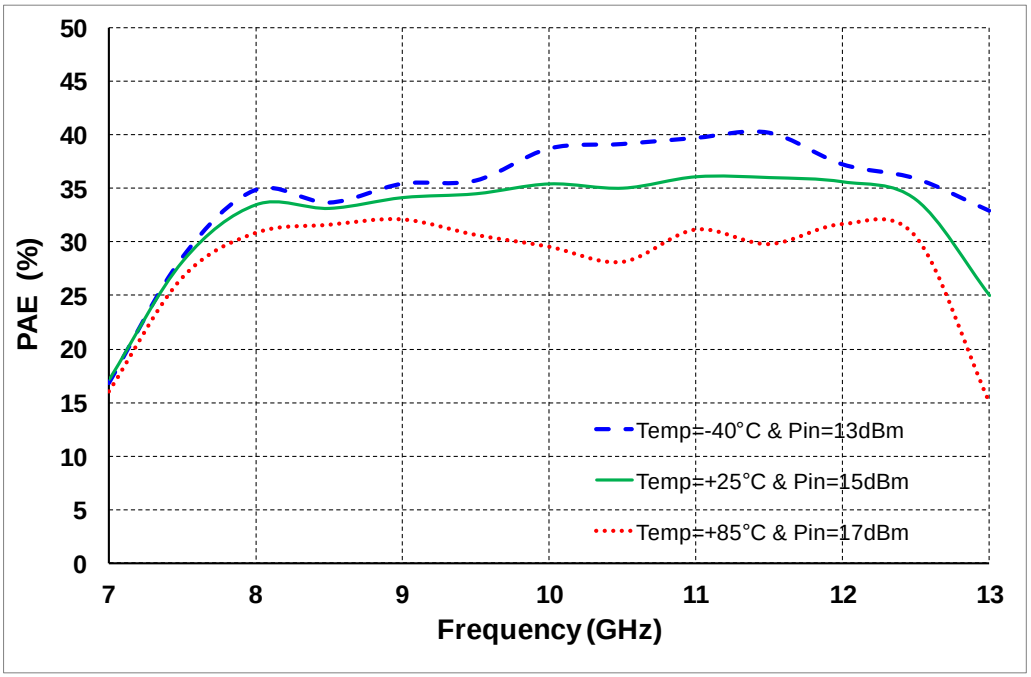
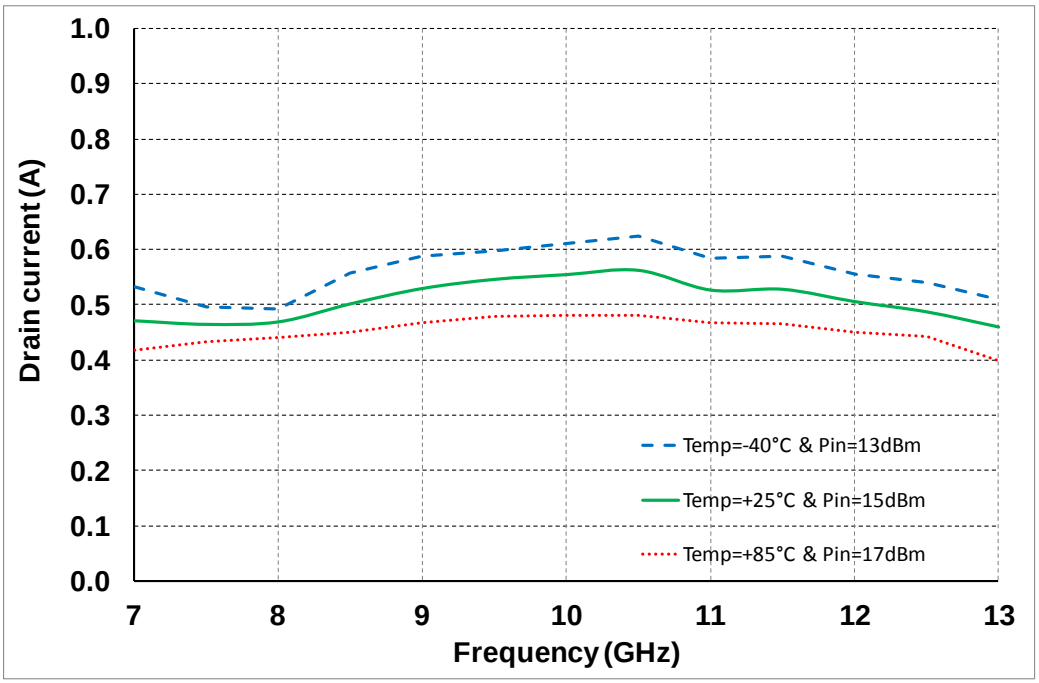
Typical Board Measurements

Temperature : -40, +25, +85°C
VD1,2 = 8V, Id (Quiescent) = 420mA, CW mode

Power added efficiency at 3dBcomp versus Frequency and Temperature



Drain current at 3 dBcomp versus Frequency and Temperature



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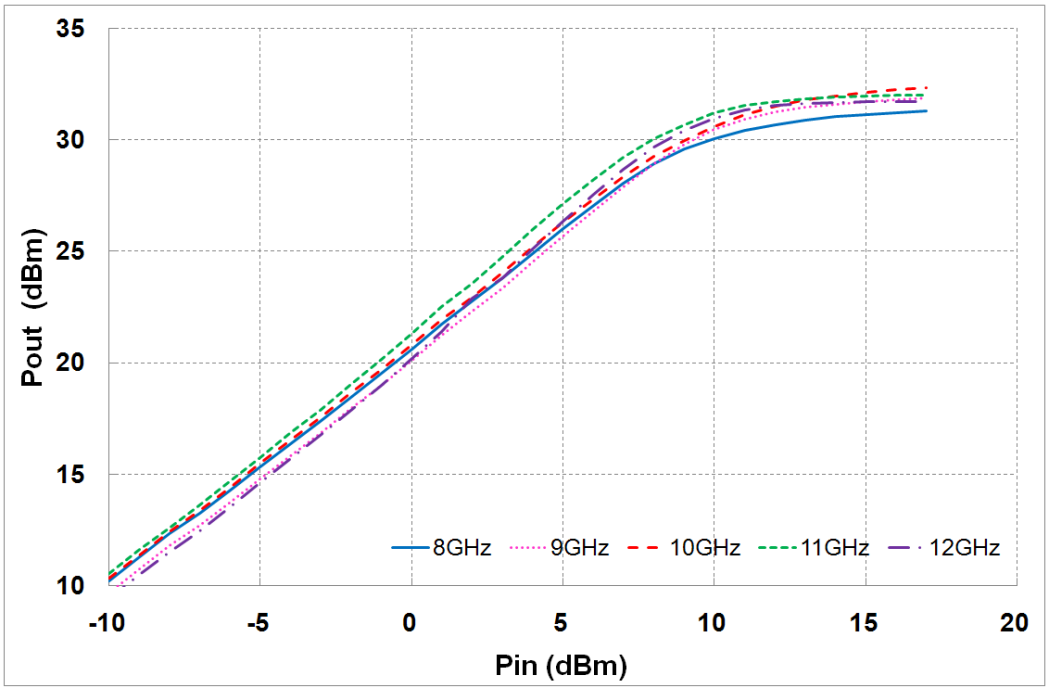
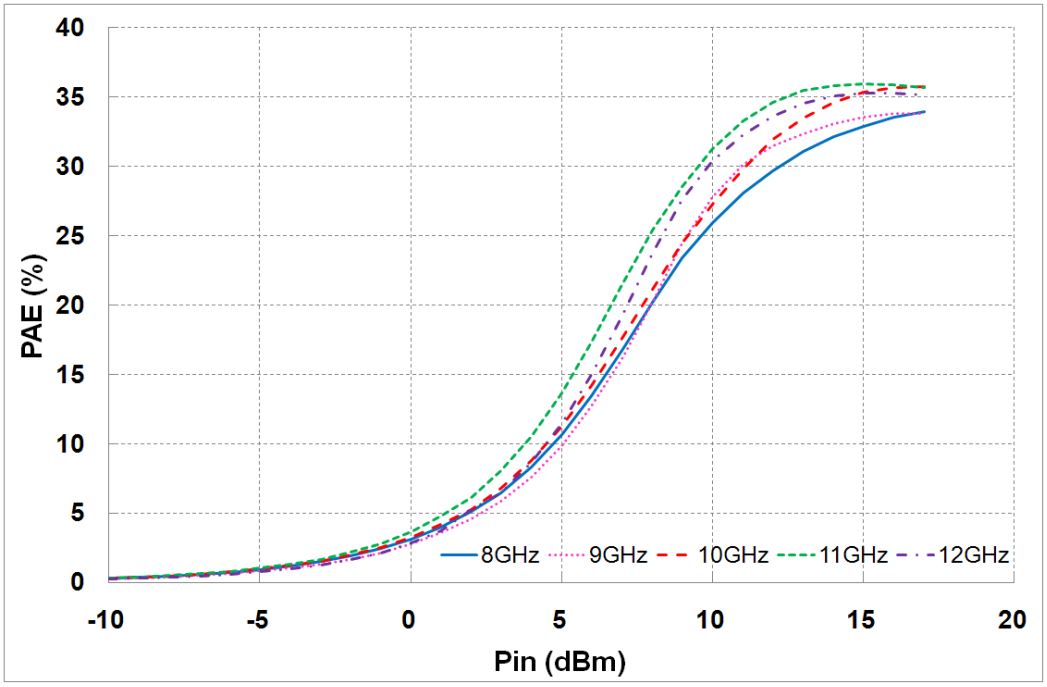
Typical Board Measurements

Temperature : +25°C
VD1,2 = 8V, Id (Quiescent) = 420mA, CW mode

Output Power versus Input Power and Frequency



Power added efficiency versus Input Power and Frequency



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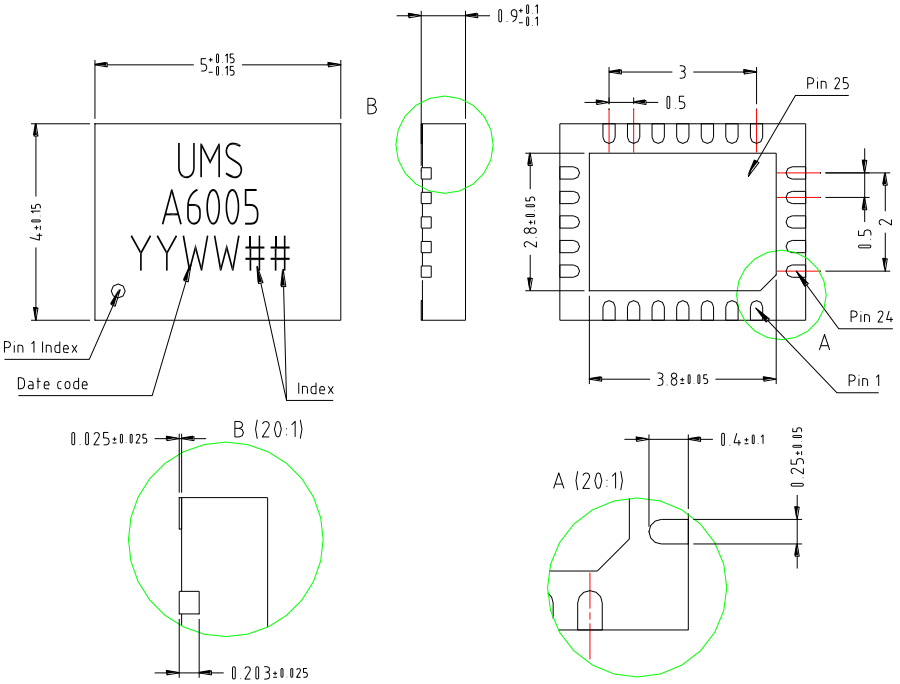
Package Outline (1)



Matt tin, Lead Free	(Green)	1- Nc	13- VD2
Units :	mm	2- Nc	14- Nc
From the standard :	JEDEC MO-220	3- Nc	15- Gnd (2)
	(VGHD)	4- Nc	16- Nc
25-	GND	5- Nc	17- VD1
		6- Nc	18- VG1
		7- Nc	19- Nc
		8- Nc	20- Nc
		9- Gnd (2)	21- Gnd (2)
		10- RF OUT	22- RF IN
		11- Gnd (2)	23- Gnd (2)
		12- Nc	24- Nc

(1) The package outline drawing included to this data-sheet is given for indication. Refer to the application note AN0017 (http://www.ums-gaas.com) for exact package dimensions.
(2) It is strongly recommended to ground all pins marked “Gnd” through the PCB board. Ensure that the PCB board is designed to provide the best possible ground to the package.

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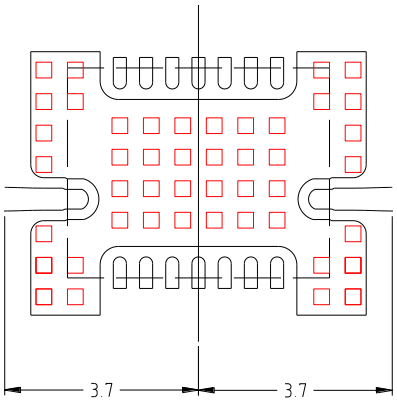
Definition of the Reference Planes

The reference planes used for measurements given above are symmetrical from the axis of the package (see drawing beside). The input and output reference planes are located at 3.7mm offset (input wise and output wise respectively) from this axis. Then, the given Sij parameters incorporate the land pattern of the evaluation motherboard recommended in paragraph "Evaluation mother board".



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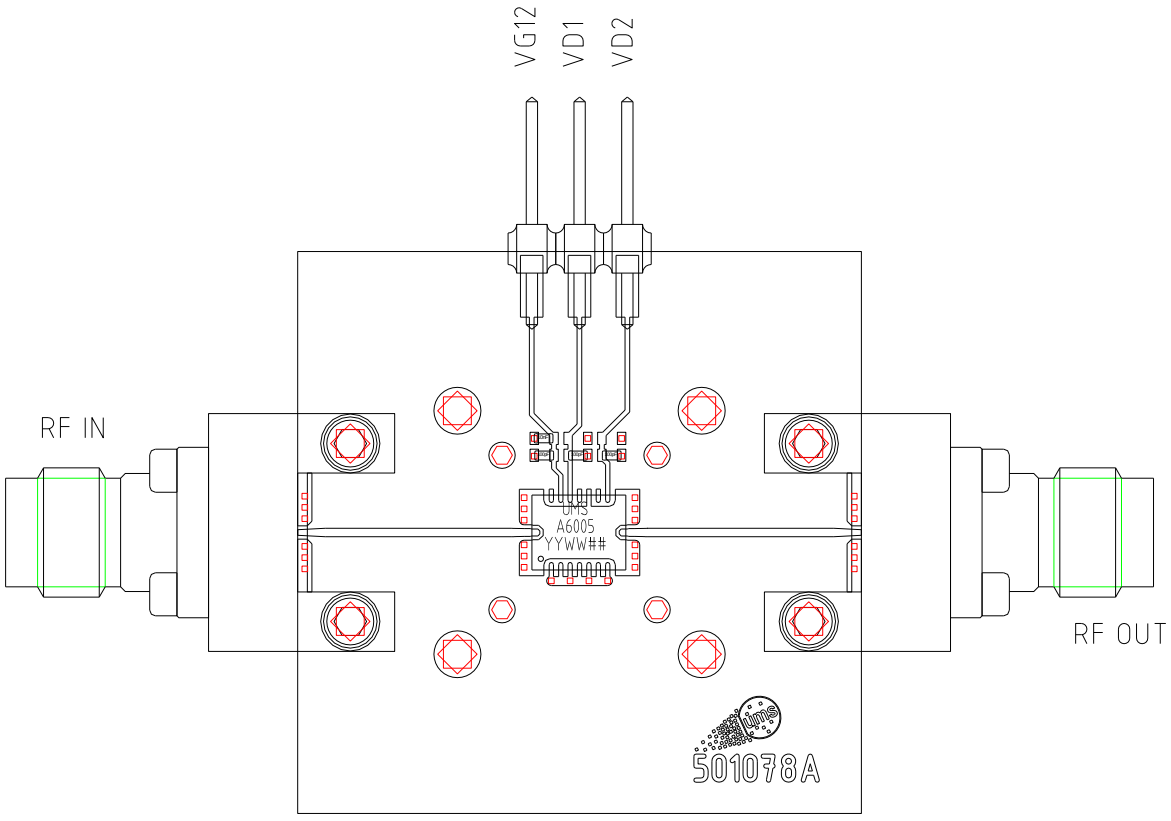
Evaluation Mother Board

- Compatible with the proposed footprint.
- Based on typically Ro4003 / 8mils or equivalent.
- Using a micro-strip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.
- Decoupling capacitors of 100pF + 10nF recommended on VG12, VD1,2 in CW mode.
- Decoupling capacitors of 100pF + 10nF recommended on VG12 in pulsed drain mode.
- Decoupling capacitors of 100pF + 10nF recommended on VD1,2 in pulsed drain mode.
- See application note AN0017 for details.

Recommended Test fixture for measurements over temperature range



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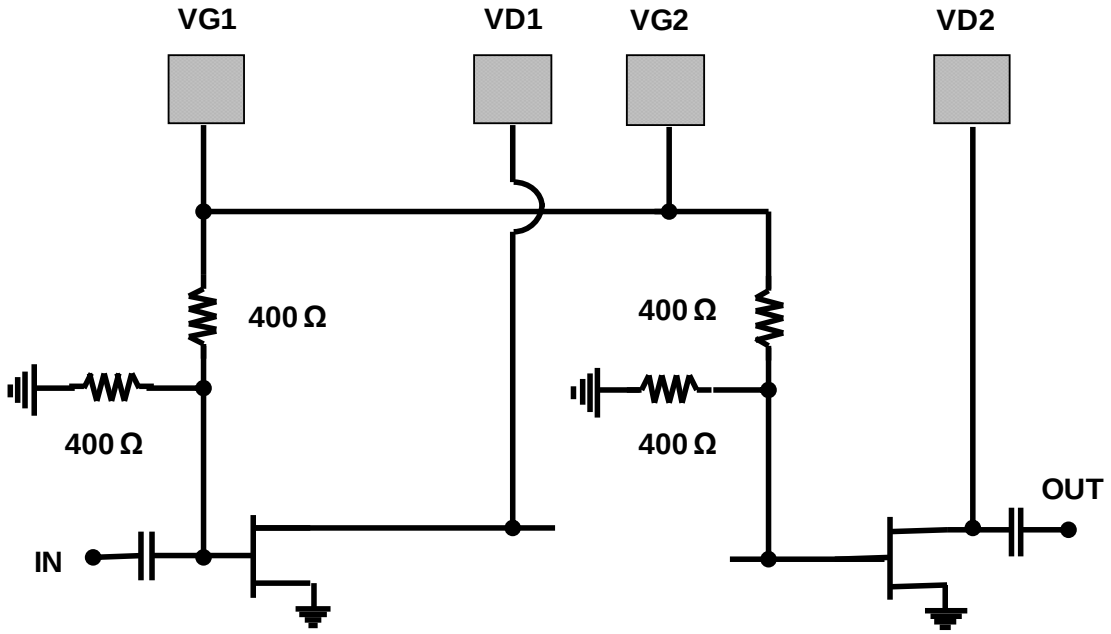
DC Schematic

8V, 420mA



Package Information

Parameter	Value
Package body material	RoHS-compliant
	Low stress Injection Molded Plastic
Lead finish	100% matte tin (Sn)
MSL Rating	MSL3

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Recommended package footprint

Refer to the application note AN0017 available at http://www.ums-gaas.com for package foot print recommendations and exact package dimensions.

SMD mounting procedure

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017 available at http://www.ums-gaas.com.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at http://www.ums-gaas.com.

Recommended ESD management

Refer to the application note AN0020 available at http://www.ums-gaas.com for ESD sensitivity and handling recommendations for the UMS package products.

Recommended thermal management

Refer to the application note AN0018 available at http://www.ums-gaas.com for thermal management recommendations.

Ordering Information

QFN Package:	CHA6005-QEG/XY	
	Stick: XY = 20	Tape & reel: XY = 21

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