

# DATA SHEET

## **PCA1070**

Multistandard programmable  
analog CMOS transmission IC

Product specification  
Supersedes data of 1996 Mar 06  
File under Integrated Circuits, IC03

1997 Jun 20

## Multistandard programmable analog CMOS transmission IC

PCA1070

### FEATURES

- Line interface with:
  - Voltage regulator with programmable DC voltage drop
  - Programmable set impedance
  - Output to control an external switching MOS transistor for pulse dialling
  - Programmable DC voltage during pulse dialling
  - Circuitry for short DC settling time
- Interface to peripheral circuits with:
  - Supply for microcontroller and DTMF diallers
  - Input to sense supply voltage of microcontroller and output for reset of microcontroller
  - I<sup>2</sup>C-bus (programming of parameters, control of all logic signals)
  - High impedance DTMF signal input
  - Input for external oscillator signal with on-chip DC blocking
  - Power-down via the I<sup>2</sup>C-bus
  - Stabilized supply for electret microphone
- Microphone and DTMF amplifiers:
  - Low-noise microphone preamplifier suitable for various types of microphones
  - Symmetrical high impedance microphone preamplifier inputs
  - Programmable gain for microphone and DTMF channels
  - Sending mute via the I<sup>2</sup>C-bus to disable microphone amplifier and enable DTMF amplifier
  - Sending mute also to be used as privacy switch
  - Dynamic limiting (speech controlled) to prevent distortion of line signal and sidetone; programmable maximum sending level
- Receiving amplifier:
  - Suitable for various types of earpieces (including piezo)
  - Programmable gain and hearing protection level
  - Receiving mute via the I<sup>2</sup>C-bus to disable receiving amplifier and enable DTMF confidence tone
  - On-chip anti-sidetone circuit with programmable sidetone balance
  - Confidence tone in the earpiece during DTMF dialling



- Facility to regulate parameters with line current:
  - Value of DC line current (bit code) readable via the I<sup>2</sup>C-bus
  - Line loss compensation with fully software programmable characteristics (control range, stop current) of microphone/earpiece/DTMF amplifiers
  - Fully software programmable control of sidetone balance and DC voltage drop as a function of line length.

### APPLICATIONS

- Wired telephony (basic till feature phones)
- Combi-terminals (e.g. telephone and answering machine or FAX)
- Modems and base units of cordless telephones.

### GENERAL DESCRIPTION

The PCA1070 is a CMOS integrated circuit performing all speech and line interface functions in fully electronic telephone sets. The device requires a minimum of external components. The transmission parameters are programmable via the I<sup>2</sup>C-bus. This makes the IC adaptable to nearly all worldwide country requirements and to a various range of speech transducers, without changing the (few) external components.

The parameters are stored in the EEPROM of a microcontroller and are loaded into the PCA1070 during the start-up phase of the transmission IC after hook-off.

The PCA1070 also allows adaptation to the connected telephone line by reading the line current via the I<sup>2</sup>C-bus and processing it in the microcontroller.

# Multistandard programmable analog CMOS transmission IC

PCA1070

## ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCA1070P	DIP24	plastic dual in-line package; 24 leads (600 mil)	SOT101-1
PCA1070T	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1

## BLOCK DIAGRAM

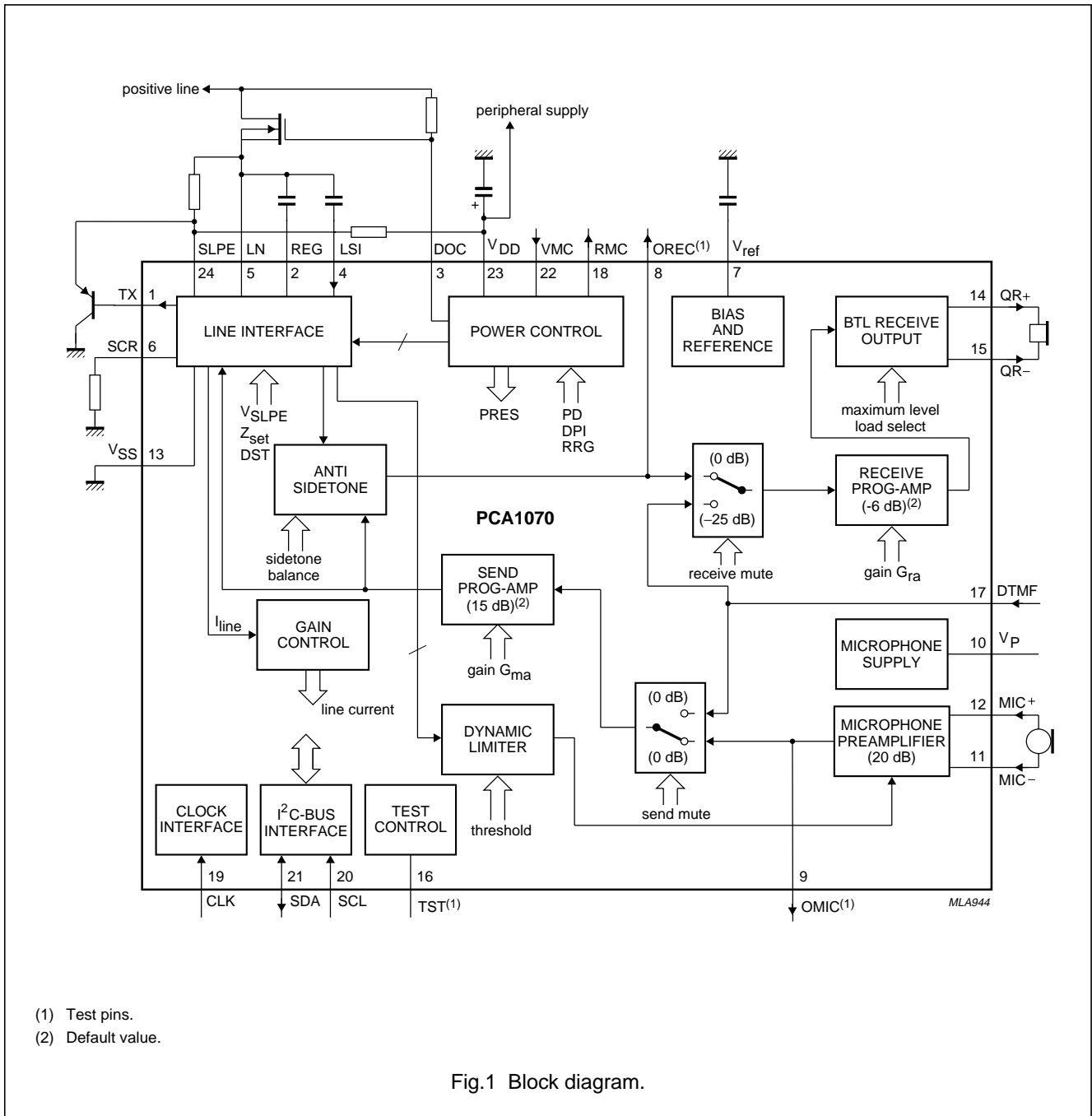


Fig.1 Block diagram.

Multistandard programmable analog  
CMOS transmission IC

PCA1070

PINNING

SYMBOL	PIN	DESCRIPTION
TX	1	drive output
REG	2	voltage regulator decoupling
DOC	3	dial output connection
LSI	4	line signal input
LN	5	positive line terminal
SCR	6	sending current resistor
V <sub>ref</sub>	7	voltage reference decoupling
OREC	8	output receiving preamplifier; to be left open-circuit in application
OMIC	9	output microphone preamplifier; to be left open-circuit in application
V <sub>P</sub>	10	supply for electret microphones
MIC-	11	inverting input microphone preamplifier
MIC+	12	non-inverting input microphone preamplifier
V <sub>SS</sub>	13	negative line terminal
QR+	14	non-inverting output of receiving amplifier
QR-	15	inverting output of receiving amplifier
TST	16	test pin; to be connected to V <sub>SS</sub> in application
DTMF	17	dual tone multi-frequency input
RMC	18	reset output for microcontroller
CLK	19	clock signal input
SCL	20	serial clock line input; I <sup>2</sup> C-bus
SDA	21	serial data line input/output; I <sup>2</sup> C-bus
VMC	22	input to sense supply voltage microcontroller
V <sub>DD</sub>	23	positive supply decoupling
SLPE	24	slope (DC resistance) adjustment

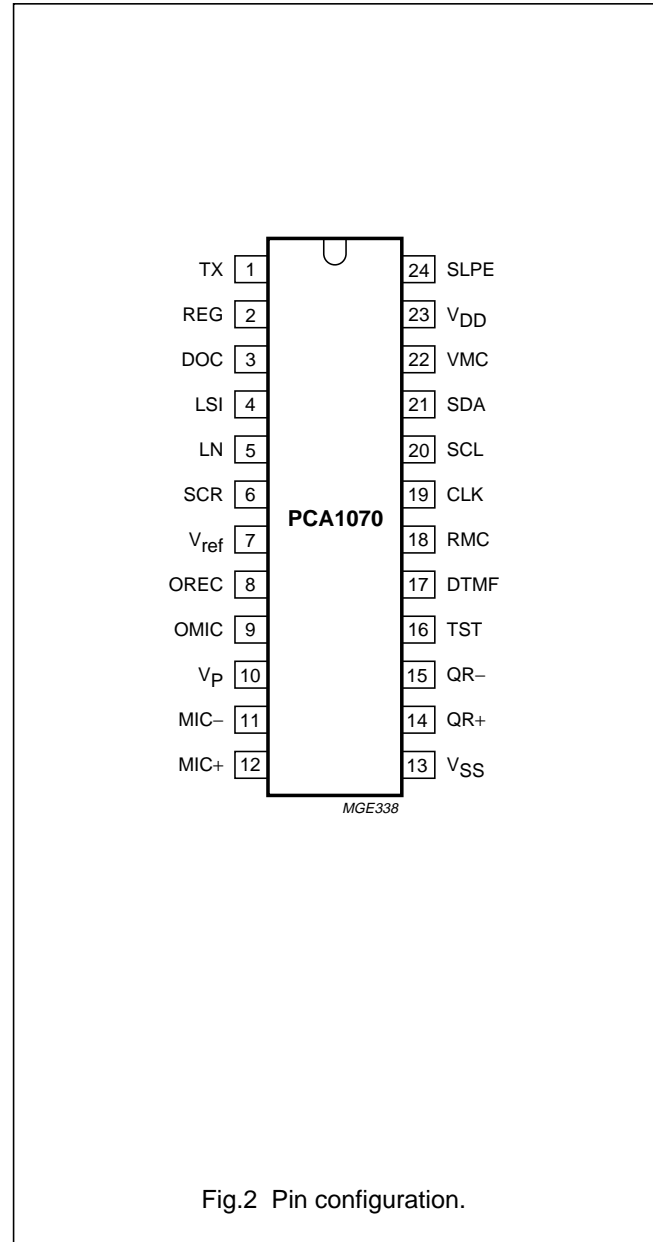


Fig.2 Pin configuration.

# Multistandard programmable analog CMOS transmission IC

PCA1070

## FUNCTIONAL DESCRIPTION

All values in the Chapter "Functional description" are typical unless stated otherwise.

### Line interface

#### DC VOLTAGE DROP

Power for the PCA1070 and its peripheral circuits is obtained from the telephone line. The IC develops its own supply voltage at  $V_{DD}$  and regulates its DC voltage drop between pins SLPE and  $V_{SS}$ . This voltage ( $V_{SLPE}$ ) can be programmed via the I<sup>2</sup>C-bus interface between 3.1 to 5.9 V and is default at 4.7 V (see Table 8).

The DC line voltage at pin LN can be calculated using the following equation:

$$V_{LN} = V_{SLPE} + (I_{line} - I_{LN}) \times R_{LN-SLPE}$$

where:

$I_{LN}$  = DC bias current flowing into pin LN  
( $\approx 3$  mA if  $I_{line} > 17$  mA)

$R_{LN-SLPE}$  = external 20  $\Omega$  resistor between LN and SLPE.

At line currents below 6 mA the DC voltage  $V_{SLPE}$  is automatically adjusted to a lower value. This means that the operation of more sets, connected in parallel, is possible with reduced sending and receiving levels and relaxed performance. At line currents below 16 mA the DC bias current  $I_{LN}$  is reduced from  $\approx 3$  mA to a lower value to ensure maximum possible transmit level capability under all line current conditions.

#### SET IMPEDANCE

In normal conditions  $I_{line} \gg I_{LN}$  and the static behaviour is equivalent to a voltage regulator diode with a series resistor  $R_{LN-SLPE}$ . In the audio frequency range the dynamic impedance  $Z_{LN}$  is determined mainly by the internal component  $Z_{set} = R_a + (R_b // C)$ . The equivalent impedance  $Z_{LN}$  is shown in Fig.3. The values of  $R_a$ ,  $R_b$  and  $C$  can be programmed via the I<sup>2</sup>C-bus interface (see Tables 9, 10 and 11).

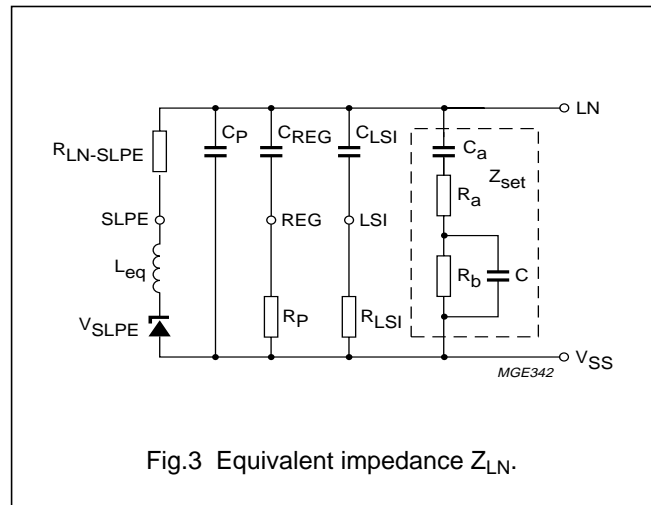


Fig.3 Equivalent impedance  $Z_{LN}$ .

where:

$C_a$  = DC blocking capacitor (influence negligible at  $f \geq 300$  Hz for given value of  $C_{LSI}$ )

$C_{LSI}$  = capacitor at pin LSI (100 nF)

$C_P$  = internal capacitor (12 nF)

$C_{REG}$  = capacitor at pin REG (470 nF)

$L_{eq}$  = artificial inductor  
( $= R_P \times R_{LN-SLPE} \times C_{REG} = 10.1$  H at  $V_{SLPE} = 4.7$  V)

$R_{LN-SLPE}$  = DC slope resistance (20  $\Omega$ )

$R_P$  = internal resistor (1075 k $\Omega$  at  $V_{SLPE} = 4.7$  V)

$R_{LSI}$  = internal resistor (240 k $\Omega$ ).

#### SUPPLY FOR PERIPHERAL CIRCUITS

The supply voltage  $V_{DD}$  can be used for peripheral circuitry. The supply capabilities depend on the programmed DC voltage drop  $V_{SLPE}$  and on several other parameters as given in the following equation:

$$V_{DD} = V_{SLPE} - (I_{DD} + I_p + I_{VP}) \times R_{SLPE-VDD}$$

where:

$I_{DD}$  = internal current consumption PCA1070 (2.3 mA)

$I_p$  = current to peripheral circuitry

$I_{VP}$  = current taken from  $V_p$  for electret microphone

$R_{SLPE-VDD}$  = external resistor between SLPE and  $V_{DD}$ .

# Multistandard programmable analog CMOS transmission IC

PCA1070

### DC STARTING AND SETTLING TIME

The IC is equipped with circuitry for fast DC start-up. This circuit is automatically activated as soon as  $V_{DD}$  reaches 3 V after hook-off, and is deactivated when  $V_{SLPE}$  drops below 5.9 V. This ensures that only a relatively short time is needed to reach the default DC setting ( $V_{SLPE}$ ) of the circuit and that  $V_{DD}$  will not exceed the maximum permitted voltage of 6 V.

The start-up circuit can also be activated under software control by setting bit code DST to logic 1 via the I<sup>2</sup>C-bus. The start-up time can be optimized by programming the bit code DST to logic 1 during the start-up procedure.

In practice this is possible as soon as the microcontroller has become operational. The DST bit can also be used to quickly restore the DC settings ( $V_{SLPE}$ ) after long line breaks or during reprogramming of  $V_{SLPE}$ .

It should be noted that the AC impedance into pin LN is reduced considerably when DST = 1.

### Power control

#### INTERNAL RESET PCA1070

The PCA1070 has an internal reset circuit that monitors the supply voltage  $V_{DD}$ . If  $V_{DD}$  is below the threshold level (1.2 V) then the circuit is in reset-mode. In this mode the current consumption is low and the internal reset is active and writes the default values into all registers. The status bit PRES will be set to logic 1. The microcontroller can read this bit via the I<sup>2</sup>C-bus interface; once read it will be set to logic 0 again.

When  $V_{DD}$  passes the threshold (increasing  $V_{DD}$ ), the circuit becomes partly active and the internal ring/speech detector will be activated (see Section "Start-up and switch-off behaviour").

#### RESET OUTPUT FOR MICROCONTROLLER

The voltage at pin VMC (microcontroller supply voltage) is monitored by a reset circuit. If  $V_{VMC}$  is below the threshold level the output RMC is set to logic 1. This threshold level is 2 V in the normal operating and power-down mode and 2.1 V in the standby mode (see Fig.4).

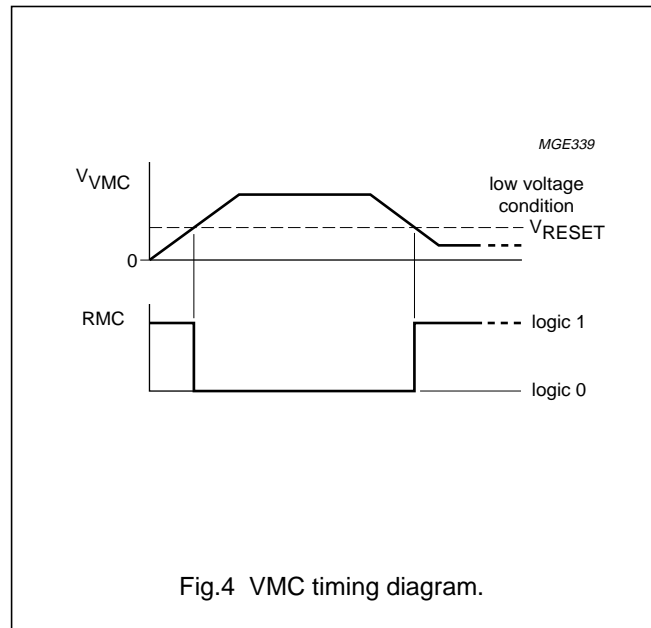


Fig.4 VMC timing diagram.

### POWER-DOWN/STANDBY MODES

The circuit can be set in power-down or standby mode. These modes are intended for use with pulse dialling during long line breaks and applications with memory retention.

With control bits PDx = 01, the circuit is in the power-down mode; the typical current consumption at pin  $V_{DD}$  is reduced from  $I_{DD} = 2.3$  mA to 30  $\mu$ A; the typical current consumption at pin VMC is 4  $\mu$ A. When PDx = 11 the circuit is in the standby mode and  $I_{DD}$  and  $I_{VMC}$  are reduced to 2  $\mu$ A. In both conditions (power-down and standby) the voltage stabilizer will be disabled.

### START-UP AND SWITCH-OFF BEHAVIOUR

This description refers to the basic application where  $V_{DD}$  and VMC are connected together and one supply capacitor is used (see Fig.8).

## Multistandard programmable analog CMOS transmission IC

PCA1070

### Speech condition

After hook-off, line current will be applied to the line input LN and the supply capacitor connected to  $V_{DD}$  and VMC will be charged.

The internal reset signal will change from logic 1 to logic 0 when  $V_{DD}$  passes the threshold level (1.2 V) and the circuit becomes partly active [the line interface part is kept in power-down mode, so that all of the line current is available to charge the supply capacitor(s)];

The PCA1070 can receive data via the I<sup>2</sup>C-bus (standard I<sup>2</sup>C specifications are fulfilled for  $V_{DD} \geq 2.5$  V; relaxed performance for  $V_{DD} = 1.8$  to 2.5 V).

When  $V_{VMC}$  passes the microcontroller reset level of 2 V (2.1 V in standby mode) the output RMC changes from logic 1 to logic 0 and the circuit is switched to the normal operating mode.

After hook-on  $V_{VMC}$  decreases and the output RMC will change from logic 0 to logic 1 when  $V_{VMC}$  passes the threshold level, however the PCA1070 will stay in the normal operating mode until the internal reset at 1.2 V takes place.

By decreasing  $V_{DD}$  the internal reset signal will change from logic 0 to logic 1 when  $V_{DD}$  passes 1.2 V and the circuit will go into the reset mode (line interface part in power-down and all programmable parameters reset to default values).

### Ringer condition

In this condition the supply capacitor connected to  $V_{DD}$  and VMC is charged by the rectified ringer signal; no line current is applied to pin LN.

$V_{DD}$  and  $V_{VMC}$  are increasing and when  $V_{DD}$  passes the internal reset threshold level (1.2 V), the internal ring/speech-detector will be activated and the circuit will switch to the standby condition ( $I_{DD} < 5 \mu\text{A}$ ;  $I_{VMC} < 5 \mu\text{A}$ ) before the voltage at VMC reaches the threshold level for microcontroller reset. When  $V_{VMC}$  passes this threshold level (2.1 V) output RMC changes from logic 1 to logic 0 and the circuit will stay in the standby mode until line current is applied to pin LN. By setting the 'Reset Ring' control bit (RRG) to logic 1 via the I<sup>2</sup>C-bus interface, the ring/speech detector will be disabled.

### DIAL PULSE INPUT (DPI)

The DPI bit controls output DOC (open-drain) that drives the gate of an external MOS interrupter transistor. DPI is controlled via the I<sup>2</sup>C-bus interface.

If DPI is set to logic 1, pin DOC will be pulled down to switch-off the MOSFET to generate a line break. If DPI = 0 pin DOC is high-ohmic and the interrupter transistor will conduct the line current.

### Sending channel

The PCA1070 has symmetrical microphone inputs and accepts input signals of maximum 70 mV (peak) for THD = 2% ( $V_{DD} \geq 2.5$  V). Its input impedance is 100 k $\Omega$  and its gain is default 41 dB. Dynamic, magnetic, piezoelectric and electret (with built-in FET source follower) microphones can be used. Some possible microphone arrangements are shown in Fig.5.

The gain of the sending channel can be programmed between 30 dB and 51 dB in 1 dB steps using bit code GMAX (6 bits). The gain of the microphone preamplifier is 20 dB (with dynamic limiter not active) and GMAX sets the gain of the 'sending prog-amp' (allowed range  $G_{ma} = 4$  to 25 dB). The gain of the line interface is 6 dB.

Thus the total gain of the sending channel ( $G_M$ ) is as follows:

$$G_M = 20 + G_{ma} + 6 \text{ (dB)}$$

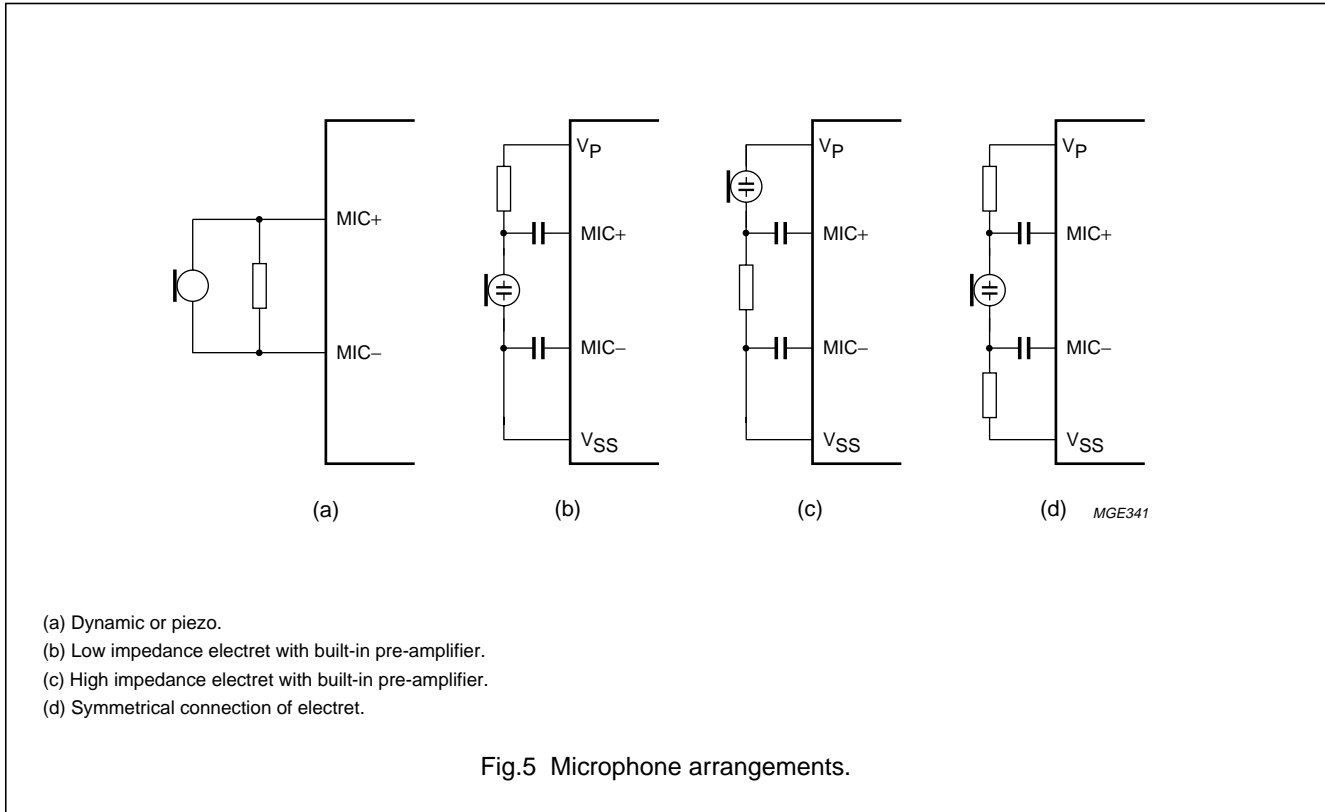
$$\text{Default: } G_M = 20 + 15 + 6 = 41 \text{ dB}$$

Where  $G_{ma}$  = 'gain sending prog-amp'.

Programming the gain of the 'sending prog-amp' is given in Table 13.

Multistandard programmable analog  
CMOS transmission IC

PCA1070



**Dynamic limiter**

To prevent distortion of the transmitted speech signal, the gain of the microphone amplifier is reduced rapidly when signal peaks on the line exceed an internally determined threshold level. The time in which the gain is reduced, the attack time, is very short. The circuit stays in this gain-reduced condition until the peaks of the sending signal remain below the threshold level. The sending gain then returns to normal after a time also determined on the chip, the release time. The threshold level of the AC peak-to-peak line voltage on pin LN is default at 3.5 V (p-p). A level of 2.6 V (p-p) can be programmed by setting bit code DLT to logic 1.

The internal threshold level is lowered automatically if the DC voltage setting of the circuit ( $V_{SLPE}$ ) is not high enough to reach the programmed level. Also when the DC current in the transmit output stage is insufficient to drive the line load, the internal threshold level is lowered automatically.

Dynamic limiting considerably improves sidetone performance in over-drive conditions (less distortion and limited sidetone level).

**DTMF channel**

The PCA1070 has an asymmetrical DTMF input. Its input impedance is  $200\text{ k}\Omega // 45\text{ pF}$  and its gain is default at 21 dB. DTMF signals can be sent to the line by setting control bit 'Sending Mute' (SM) to logic 1 (default SM = 0); by setting 'Receiving Mute' (RM) also to logic 1 (default RM = 0), the dialling tones are also sent to the receiving output to generate a confidence tone in the earpiece.

The gain between the DTMF input and the line LN can be programmed between 1 dB and 21 dB in 1 dB steps using bit code GMAx (6 bits). The confidence tone gain (between DTMF input and earpiece outputs QR) can be programmed between -40 dB and -19 dB (symmetrical drive of earpiece) using bit code GRAx (6 bits). GMAx sets the gain of the 'sending prog-amp' (recommended range in DTMF mode for  $G_{ma} = -5$  to 15 dB) and GRAx sets the gain of the 'rec prog-amp' (allowed range  $G_{ra} = -25$  to 0 dB).



# Multistandard programmable analog CMOS transmission IC

PCA1070

The total gain of the DTMF channel between the DTMF input and the line LN is as follows:

$$G_{\text{DTMF}} = G_{\text{ma}} + 6 \text{ (dB)}$$

$$\text{Default } G_{\text{DTMF}} = 15 + 6 = 21 \text{ dB}$$

The confidence tone gain (DTMF to QR outputs) is:

With symmetrical drive of earpiece  $G_{\text{CTS}} = G_{\text{ra}} - 19 \text{ (dB)}$

$$\text{Default } G_{\text{CTS}} = -6 - 19 = -25 \text{ dB.}$$

At low gain settings ( $G_{\text{ra}} < -10 \text{ dB}$ ), the confidence tone gain will be slightly higher than the calculated value. This is caused by a residual signal.

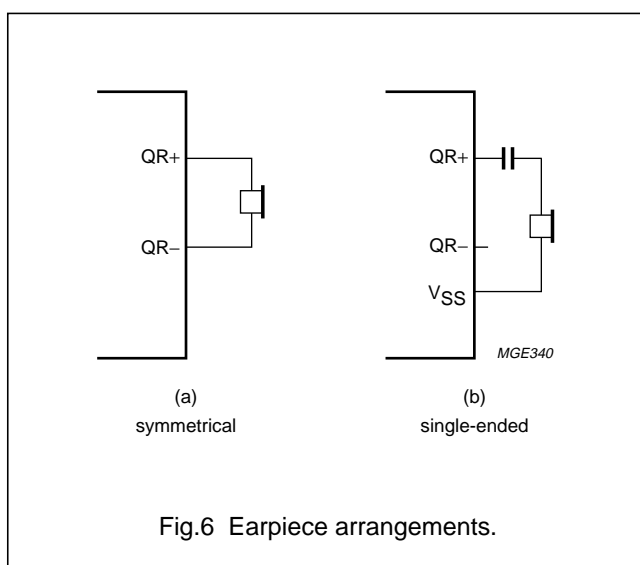
Programming the gain of the 'sending prog-amp' and the 'rec prog-amp' is given in Table 13.

## Receiving channel

The gain of the receiving channel is defined between the line connection LN and the earpiece outputs QR+ and QR-. Its voltage gain is default  $-6 \text{ dB}$  (differential drive). The LN terminal accepts receiving signals up to  $1 \text{ V (RMS)}$  for  $\text{THD} = 2\%$ . The outputs may be used to connect dynamic, magnetic or piezoelectric earpieces with single-ended or differential drive. The load select bit RFC is set default to logic 1 to guarantee stable operation in case of a capacitive load (piezoelectric earpiece). With a resistive load (dynamic capsule) RFC should be set to logic 0 via the I<sup>2</sup>C-bus interface to obtain optimum performance with respect to distortion and bandwidth.

Two levels for hearing protection can be selected via the I<sup>2</sup>C-bus interface with control bit HPL.

The earpiece arrangements are illustrated in Fig.6.



The gain of the receiving channel can be programmed between  $-19 \text{ dB}$  and  $+11 \text{ dB}$  (symmetrical drive) in  $1 \text{ dB}$  steps using bit code GRAX (6 bits).

GRAX sets the gain of the 'rec prog-amp' (allowed range  $G_{\text{ra}} = -19 \text{ dB}$  to  $+11 \text{ dB}$ ; default  $G_{\text{ra}} = -6 \text{ dB}$ ).

The total gain of the receiving channel is as follows:

$$\text{Symmetrical drive } G_{\text{RS}} = G_{\text{ra}} \text{ (dB)}$$

$$\text{Default } G_{\text{RS}} = -6 \text{ dB.}$$

Asymmetrical or single-ended drive  $G_{\text{RA}} = G_{\text{RS}} - 6 \text{ (dB)}$

$$\text{Default } G_{\text{ra}} = -6 - 6 \text{ (dB)} = -12 \text{ dB.}$$

Programming the gain  $G_{\text{ra}}$  of the 'rec prog-amp' is given in Table 13.

## Sidetone balance

The PCA1070 has an on-chip anti-sidetone circuit. An internal balance impedance  $Z_{\text{oss}}$  can be programmed via the I<sup>2</sup>C-bus interface to match the external line impedance  $Z_{\text{line}}$  to give optimum sidetone suppression.

$$Z_{\text{oss}} = R_{\text{sa}} + (R_{\text{sb}} // C_{\text{s}}).$$

Programming the sidetone balance impedance is given in Tables 14, 15 and 16.

## Line current control

The DC line current can be read via the I<sup>2</sup>C-bus interface. This information can be used for the adaptation of transmission parameters (for example line loss compensation, sidetone balance and DC characteristic).

The bit code LCx as a function of line current is given in Table 17.

# Multistandard programmable analog CMOS transmission IC

PCA1070

## I<sup>2</sup>C-BUS PROGRAMMING

**Table 1** Programmable parameters

The following parameters (see Fig.1) can be programmed by means of a bit code via the I<sup>2</sup>C-bus:

SYMBOL	PARAMETER	BLOCK	BITS	DESCRIPTION
VDCx	V <sub>SLPE</sub>	line interface	3	DC voltage SLPE-V <sub>SS</sub>
ZSAx	set impedance	line interface	3	R <sub>a</sub> of set impedance
ZSBx		line interface	3	R <sub>b</sub> of set impedance
ZSPx		line interface	4	f <sub>p</sub> (pole frequency) of set impedance
DST	DST	line interface	1	DC Start Time
PDx	PD	power control	2	Power-Down
DPI	DPI	power control	1	Dial Pulse Input
RRG	RRG	power control	1	Reset RinG detector
HPL	maximum receiving level	BTL receiving output	1	Hearing Protection Level
RFC	load select	BTL receiving output	1	Resistive/Capacitive load
ZOSAx	sidetone impedance	anti-sidetone	4	R <sub>sa</sub> of sidetone impedance
ZOSBx		anti-sidetone	4	R <sub>sb</sub> of sidetone impedance
ZOSPx		anti-sidetone	4	C <sub>s</sub> of sidetone impedance
RM	receiving mute	receiving mute	1	Receiving Mute
GRAx	gain G <sub>ra</sub>	receiving prog-amp	6	Gain receiving prog-amp
GMAx	gain G <sub>ma</sub>	sending prog-amp	6	Gain sending prog-amp
SM	sending mute	sending mute	1	Sending Mute
DLT	threshold	dynamic limiter	1	Dynamic Limiter Threshold

**Table 2** Readable parameters

The following parameters (see also Fig.1) can be read as a bit code via the I<sup>2</sup>C-bus:

SYMBOL	PARAMETER	BLOCK	BITS	DESCRIPTION
PRES	PRES	power control	1	PCA1070 Reset
LCx	line current	gain control	5	Line Current

## I<sup>2</sup>C interface

The I<sup>2</sup>C-bus interface (see "The I<sup>2</sup>C-bus and how to use it" 12NC: 9398 393 40011) is used to program the transmission parameters and control functions.

**Table 3** Device address

A6	A5	A4	A3	A2	A1	A0	R/W
0	1	0	0	0	1	0	X

All functions can be accessed by writing an 8-bit word to the PCA1070. In order to set up the PCA1070, a control message consisting of the device address, a R/W bit, a subaddress byte and one or more data bytes must be written to the PCA1070. If more than one data byte follows the subaddress, these bytes are stored in the successive registers by the automatic increment feature.

Multistandard programmable analog  
CMOS transmission IC

PCA1070

**Table 4** The control word format for the slave receiver

DEVICE ADDRESS										SUB ADDRESS								DATA/CONTROL BYTE											
S	0	1	0	0	0	1	0	0 <sup>(1)</sup>	A	A	17	16	15	14	13	12	11	10	A	D7	D6	D5	D4	D3	D2	D1	D0	A	P

**Note**

1. This bit is  $R/\overline{W}$ .

**Table 5** Bit arrangement of each data byte used in the control word: PCA1070 receive (see note 1)

FUNCTION	SUB ADDRESS	D7	D6	D5	D4	D3	D2	D1	D0
DC voltage	H00		VDC2	VDC1	VDC0				DST
Sidetone and set impedance	H01	ZOSB3	ZOSB2	ZOSB1	ZOSB0	ZOSA3	ZOSA2	ZOSA1	ZOSA0
	H02	ZOSP3	ZOSP2	ZOSP1	ZOSP0		ZSA2	ZSA1	ZSA0
	H03		ZSB2	ZSB1	ZSB0	ZSP3	ZSP2	ZSP1	ZSP0
Sending channel	H04	DLT		GMA5	GMA4	GMA3	GMA2	GMA1	GMA0
Receiving channel	H05	RFC	HPL	GRA5	GRA4	GRA3	GRA2	GRA1	GRA0
Control	H06	PD1	PD0		RRG	RM	SM		DPI

**Note**

1. The bits that are not indicated must be set to logic 0.

**Table 6** The control word format for the slave transmitter

DEVICE ADDRESS										DATA/STATUS BYTE									
S	0	1	0	0	0	1	0	1 <sup>(1)</sup>	A	D7	D6	D5	D4	D3	D2	D1	D0	A	P

**Note**

1. Change in direction of  $R/\overline{W}$  bit.

**Table 7** PCA1070 send

FUNCTION	D7	D6	D5	D4	D3	D2	D1	D0
PCA1070 status	PRES <sup>(1)</sup>	–	–	LC4 <sup>(2)</sup>	LC3 <sup>(2)</sup>	LC2 <sup>(2)</sup>	LC1 <sup>(2)</sup>	LC0 <sup>(2)</sup>

**Notes**

1. Indicates if PCA1070 has received internal reset; PRES will be set to logic 1 with internal reset and is set to logic 0 after reading the register via the I<sup>2</sup>C-bus.
2. Information about value of line current.

# Multistandard programmable analog CMOS transmission IC

PCA1070

## WRITE AND READ TABLES

### DC voltages

**Table 8** DC voltage at pin SLPE

VDC2	VDC1	VDC0	V <sub>SLPE</sub> (V)	REMARK
0	0	0	3.1	
0	0	1	3.5	
0	1	0	3.9	
0	1	1	4.3	
<b>1</b>	<b>0</b>	<b>0</b>	<b>4.7</b>	<b>default</b>
1	0	1	5.1	
1	1	0	5.5	
1	1	1	5.9	

### Set impedance

Programming the impedance in the audio frequency range seen at pin LN:  $R_a + (R_b // C)$

**Table 9** Programming  $R_a$

ZSA2	ZSA1	ZSA0	$R_a$ ( $\Omega$ )	REMARK
0	0	0	0	
0	0	1	100	
<b>0</b>	<b>1</b>	<b>0</b>	<b>200</b>	<b>default</b>
0	1	1	300	
1	0	0	400	
1	0	1	500	note 1
1	1	X	600	notes 1 and 2

### Notes

- For  $Z_{set}$  combinations where  $R_a = 0$  only  $R_b = 600 \Omega$  is allowed. If  $R_a \geq 500 \Omega$  it is obligatory that  $R_b = 0$ . This is to safeguard stable operation of the line interface under all practical conditions. If  $Z_{ref}$  requires  $R_a = 0$  and  $R_b \neq 600 \Omega$  use  $R_a = 100 \Omega$  instead and reduce the original  $R_b$  by  $100 \Omega$ .
- X = don't care.

# Multistandard programmable analog CMOS transmission IC

PCA1070

**Table 10** Programming  $R_b$ 

ZSB2	ZSB1	ZSB0	$R_b$ ( $\Omega$ )	REMARK
0	0	0	0	note 1
0	0	1	600	
0	1	0	700	
<b>0</b>	<b>1</b>	<b>1</b>	<b>800</b>	<b>default</b>
1	X	0	900	note 2
1	X	1	1000	note 2

**Notes**

- For  $Z_{set}$  combinations where  $R_a = 0$  only  $R_b = 600 \Omega$  is allowed. If  $R_a \geq 500 \Omega$  it is obligatory that  $R_b = 0$ . This is to safeguard stable operation of the line interface under all practical conditions. If  $Z_{ref}$  requires  $R_a = 0$  and  $R_b \neq 600 \Omega$  use  $R_a = 100 \Omega$  instead and reduce the original  $R_b$  by  $100 \Omega$ .
- X = don't care.

**Table 11** Programming pole frequency:

ZSP3	ZSP2	ZSP1	ZSP0	$f_p$ (Hz)	CORRESPONDING VALUE OF C (nF) <sup>(1)</sup>					REMARK
					$R_b$ (600 $\Omega$ )	$R_b$ (700 $\Omega$ )	$R_b$ (800 $\Omega$ )	$R_b$ (900 $\Omega$ )	$R_b$ (1000 $\Omega$ )	
0	0	0	0	828	320	275	240	214	192	
0	0	0	1	1095	242	207	182	161	145	
0	0	1	0	1448	183	157	137	122	110	
<b>0</b>	<b>0</b>	<b>1</b>	<b>1</b>	<b>1915</b>	<b>139</b>	<b>119</b>	<b>104</b>	<b>92</b>	<b>83</b>	<b>default</b>
0	1	0	0	2533	105	90	79	70	63	
0	1	0	1	3350	79	68	59	53	48	
0	1	1	0	4430	60	51	45	40	36	
0	1	1	1	5859	45	39	34	30	27	
1	X	X	X	12000	22	19	17	15	13	note 2

**Notes**

- $C = \frac{1}{2\pi \times R_b \times f_p}$
- X = don't care.

**Reset functions**

Monitoring of internal reset PCA1070.

**Table 12** Status bit PRES

PRES	DESCRIPTION
1	internal reset has occurred; default values in all registers
0	register has been read via the I <sup>2</sup> C-bus interface

# Multistandard programmable analog CMOS transmission IC

PCA1070

## Programmable amplifier (prog-amp)

An identical programmable amplifier called 'prog-amp' is used both in the sending and receiving channel. The bit codes GMAx and GRAx are given in Table 13. The permitted adjustment range differs for the two amplifiers and is also different for DTMF and speech mode. This is indicated in the corresponding sections.

**Table 13** Bit code prog-amp

GAIN (dB)	GMA5	GMA4	GMA3	GMA2	GMA1	GMA0
	GRA5	GRA4	GRA3	GRA2	GRA1	GRA0
-25	1	1	1	0	0	1
-24	1	1	1	0	0	0
-23	1	1	0	1	1	1
-22	1	1	0	1	1	0
-21	1	1	0	1	0	1
-20	1	1	0	1	0	0
-19	1	1	0	0	1	1
-18	1	1	0	0	1	0
-17	1	1	0	0	0	1
-16	1	1	0	0	0	0
-15	1	0	1	1	1	1
-14	1	0	1	1	1	0
-13	1	0	1	1	0	1
-12	1	0	1	1	0	0
-11	1	0	1	0	1	1
-10	1	0	1	0	1	0
-9	1	0	1	0	0	1
-8	1	0	1	0	0	0
-7	1	0	0	1	1	1
<b>-6<sup>(1)</sup></b>	<b>1</b>	<b>0</b>	<b>0</b>	<b>1</b>	<b>1</b>	<b>0</b>
-5	1	0	0	1	0	1
-4	1	0	0	1	0	0
-3	1	0	0	0	1	1
-2	1	0	0	0	1	0
-1	1	0	0	0	0	1
-0	1	0	0	0	0	0

GAIN (dB)	GMA5	GMA4	GMA3	GMA2	GMA1	GMA0
	GRA5	GRA4	GRA3	GRA2	GRA1	GRA0
+0	0	0	0	0	0	0
+1	0	0	0	0	0	1
+2	0	0	0	0	1	0
+3	0	0	0	0	1	1
+4	0	0	0	1	0	0
+5	0	0	0	1	0	1
+6	0	0	0	1	1	0
+7	0	0	0	1	1	1
+8	0	0	1	0	0	0
+9	0	0	1	0	0	1
+10	0	0	1	0	1	0
+11	0	0	1	0	1	1
+12	0	0	1	1	0	0
+13	0	0	1	1	0	1
+14	0	0	1	1	1	0
<b>+15<sup>(2)</sup></b>	<b>0</b>	<b>0</b>	<b>1</b>	<b>1</b>	<b>1</b>	<b>1</b>
+16	0	1	0	0	0	0
+17	0	1	0	0	0	1
+18	0	1	0	0	1	0
+19	0	1	0	0	1	1
+20	0	1	0	1	0	0
+21	0	1	0	1	0	1
+22	0	1	0	1	1	0
+23	0	1	0	1	1	1
+24	0	1	1	0	0	0
+25	0	1	1	0	0	1

### Notes

1. Default value 'rec prog-amp' GRAx.
2. Default value 'sending prog-amp' GMAx.

# Multistandard programmable analog CMOS transmission IC

PCA1070

### Sidetone balance impedance

Internal balance impedance  $Z_{oss}$  to match the external line impedance  $Z_{line}$  to give optimum sidetone suppression.

$$Z_{oss} = R_{sa} + (R_{sb} // C_s).$$

The optimum setting of  $R_{sa}$  depends on the value of the set impedance. To safeguard stable operation of the anti-sidetone circuit under all practical conditions, the following condition must be fulfilled:  $R_{sa} \geq 0.5R_a$ .

**Table 14** Programming  $R_{sa}$

ZOSA3	ZOSA2	ZOSA1	ZOSA0	$R_{sa}$ ( $\Omega$ )
0	0	0	0	134
0	0	0	1	153
0	0	1	0	193
0	0	1	1	221
0	1	0	0	246
0	1	0	1	277
0	1	1	0	295
0	1	1	1	341
1	0	0	0	369
1	0	0	1	443
<b>1</b>	<b>0</b>	<b>1</b>	<b>0</b>	<b>492<sup>(1)</sup></b>
1	0	1	1	–
1	1	0	0	–
1	1	0	1	–
1	1	1	0	–
1	1	1	1	–

**Note**

- 1. Default value.

**Table 15** Programming  $R_{sb}$

MSB	ZOSB		LSB	$R_{sb}$ ( $\Omega$ )
0	0	0	0	465
0	0	0	1	637
0	0	1	0	710
0	0	1	1	803
0	1	0	0	893
0	1	0	1	1003
<b>0</b>	<b>1</b>	<b>1</b>	<b>0</b>	<b>1259<sup>(1)</sup></b>
0	1	1	1	1410
1	0	0	0	1572
1	0	0	1	1773
1	0	1	0	1978
1	0	1	1	2216
1	1	0	0	–
1	1	0	1	–
1	1	1	0	–
1	1	1	1	–

**Note**

- 1. Default value.

**Table 16** Programming  $C_s$

MSP	ZOSP			$C_s$ (nf)
			LSP	
0	0	0	0	5
0	0	0	1	55
0	0	1	0	58
0	0	1	1	69
0	1	0	0	76
0	1	0	1	85
0	1	1	0	96
0	1	1	1	105
1	0	0	0	121
<b>1</b>	<b>0</b>	<b>0</b>	<b>1</b>	<b>134<sup>(1)</sup></b>
1	0	1	0	145
1	0	1	1	166
1	1	0	0	186
1	1	0	1	207
1	1	1	0	232
1	1	1	1	259

**Note**

- 1. Default value.

# Multistandard programmable analog CMOS transmission IC

PCA1070

## Line current control

**Table 17** Bit code LCx and DC line current

LC4	LC3	LC2	LC1	LC0	I <sub>line</sub> (typ.) (mA)
0	0	0	0	0	<12.5
0	0	0	0	1	15.0
0	0	0	1	0	17.5
0	0	0	1	1	20.0
0	0	1	0	0	22.5
0	0	1	0	1	25.0
0	0	1	1	0	27.5
0	0	1	1	1	30.0
0	1	0	0	0	32.5
0	1	0	0	1	35.0
0	1	0	1	0	37.5
0	1	0	1	1	40.0
0	1	1	0	0	42.5
0	1	1	0	1	45.0
0	1	1	1	0	47.5
0	1	1	1	1	50.0
1	0	0	0	0	52.5
1	0	0	0	1	55.0
1	0	0	1	0	58.0
1	0	0	1	1	61.0
1	0	1	0	0	64.0
1	0	1	0	1	66.5
1	0	1	1	0	69.0
1	0	1	1	1	71.5
1	1	0	0	0	74.0
1	1	0	0	1	77.5
1	1	0	1	0	80.0
1	1	0	1	1	82.5
1	1	1	0	0	85.0
1	1	1	0	1	88.0
1	1	1	1	0	91.0
1	1	1	1	1	>94.0



# Multistandard programmable analog CMOS transmission IC

PCA1070

## LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
$V_{LN}$	positive line voltage at pin LN	-0.8	+12	V
$V_i$	input voltage on pins SLPE, DOC, REG, TX and LSI	-0.8	+12	V
$V_{DD}$	supply voltage	-0.8	+7.0	V
$V_n$	voltage on all other pins	-0.8	+7.0	V
$I_i$	input current	-10	+10	mA
$P_{tot}$	total power dissipation	-	250	mW
$T_{stg}$	storage temperature	-40	+125	°C
$T_{amb}$	operating ambient temperature	-10	+60	°C

## HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

## THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient in free air		
	DIP24	54	K/W
	SO24	74	K/W

# Multistandard programmable analog CMOS transmission IC

PCA1070

## TEST CONDITIONS AND PARAMETER SETTINGS FOR THE CHARACTERISTICS

**Table 18** Test conditions

SYMBOL	VALUE	UNIT
$I_{line}$	20	mA
$V_{SS}$	0	V
$f$	1000	Hz
$I_p$	0	A
$I_{VP}$	0	A
$f_{clk}$	3.597545	MHz
$T_{amb}$	25	°C
$Z_{line}$	220 $\Omega$ + 820 $\Omega$ // 115 nF	
$R_m$	150	$\Omega$
$R_t$	150	$\Omega$

**Table 19** Test settings and control bits. All values, except RFC, are default. Programmable via the I<sup>2</sup>C-bus; bit codes are given in Chapter "I<sup>2</sup>C-bus programming".

SYMBOL	VALUE
VDCx	100
ZSAx	010
ZSBx	011
ZSPx	0011
GMAx	001111
GRAx	100110
ZOSAx	1010
ZOSBx	0110
ZOSPx	1001
DST	0
DLT	0
RFC	0
HPL	0
PDx	00
RRG	0
RM	0
SM	0
DPI	0

# Multistandard programmable analog CMOS transmission IC

PCA1070

## CHARACTERISTICS

All parameters are measured in the test circuit of Fig.7 under the conditions specified in Tables 18 and 19; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>DC line interface: LN, TX, SLPE and REG</b>						
$I_{line}$	line current operating range		17	–	140	mA
		reduced sending level	12	–	17	mA
$V_{SLPE}$	DC voltage at SLPE	with or without clock	4.3	4.7	5.1	V
$V_{SLPE(min)}$	minimum selectable value	$V_{DCx} = 000$	2.8	3.1	3.4	V
$V_{SLPE(max)}$	maximum selectable value	$V_{DCx} = 111$	5.4	5.9	6.4	V
$V_{SLPE(step)}$	step resolution		–	0.4	–	V
$V_{SLPE}$	DC voltage at SLPE	with or without clock; fast start-up; DST = 1	–	4.7	–	V
$V_{SLPE(min)}$	minimum selectable value	fast start-up; DST = 1; $V_{DCx} = 000$	–	3.1	–	V
$V_{SLPE(max)}$	maximum selectable value	fast start-up; DST = 1; $V_{DCx} = 111$	–	5.9	–	V
$V_{SLPE(step)}$	step resolution	fast start-up; DST = 1	–	0.4	–	V
$\Delta V_{SLPE}$	variation with temperature	at $T_{amb} = -10\text{ }^{\circ}\text{C}$ to $+60\text{ }^{\circ}\text{C}$ with respect to $25\text{ }^{\circ}\text{C}$	–	$\pm 20$	–	mV
$V_{LN}$	DC line voltage at LN	with or without clock	4.6	5.0	5.4	V
		$I_{line} = 12\text{ mA}$		4.83		V
		$I_{line} = 120\text{ mA}$	6.5	7.0	7.5	V
$V_{LN}$	DC line voltage at LN at low line current	with or without clock; $I_{line} = 0.25\text{ mA}$	–	1	–	V
		$I_{line} = 2\text{ mA}$	–	1.9	–	V
		$I_{line} = 4\text{ mA}$	–	3.4	–	V
		$I_{line} = 7\text{ mA}$	–	4.73	5.2	V
$t_{DC}$	DC start-up time	$C_{VDD} = 470\text{ }\mu\text{F}$ ; no clock; note 1	–	145	–	ms
<b>TX: DRIVE OUTPUT FOR EXTERNAL PNP</b>						
$V_{TX}$	output voltage at TX	external PNP disconnected; $V_{SLPE} = 2\text{ V}$ ; $V_{REG} = 1.5\text{ V}$ ; $V_{DD} = V_{VMC} = 2.5\text{ V}$ ; $I_{TX} = 0\text{ mA}$	–	1.45	–	V
		$V_{SLPE} = 3\text{ V}$ ; $V_{REG} = 2.5\text{ V}$ ; $V_{DD} = V_{VMC} = 2.5\text{ V}$ ; $I_{TX} = 1.6\text{ mA}$	–	2.2	–	V
$t_{sw}$	switching time DC voltage at SLPE	$V_{SLPE}$ steps from 3.1 V to 5.9 V; note 2	–	65	–	ms
		$V_{SLPE}$ steps from 5.9 V to 3.1 V; note 2	–	65	–	ms
		fast start-up; DST = 1; $V_{SLPE}$ steps from 3.1 V to 5.9 V; note 2	–	0.5	–	ms
		fast start-up; DST = 1; $V_{SLPE}$ steps from 5.9 V to 3.1 V; note 2	–	1	–	ms

# Multistandard programmable analog CMOS transmission IC

PCA1070

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Supplies: <math>V_{DD}</math>, <math>V_{MC}</math>, <math>V_P</math> and <math>SLPE</math></b>						
$V_{DD}$	operating supply voltage	note 3	2.5	–	6	V
		relaxed performance; note 4	1.8	–	2.5	V
$V_{DD}$ : SUPPLY PIN						
$I_{DD}$	internal current consumption	$V_{DD} = 2.5$ V	–	2.3	–	mA
		power-down; PDx = 01; SCL = 1; SDA = 1	–	30	100	$\mu$ A
		standby; PDx = 11; SCL = 1; SDA = 1	–	2	5	$\mu$ A
$V_{DD}$ : PERIPHERAL SUPPLY						
$I_p$	current available for peripheral circuitry	$V_{DD} = 2.9$ V; RM = 1; SM = 1	–	4.9	–	mA
		$V_{DD} = 2.5$ V; RM = 1; SM = 1	–	6.5	–	mA
<b><math>V_{MC}</math>: SENSE INPUT MICROCONTROLLER SUPPLY VOLTAGE</b>						
$I_{VMC}$	input current	$V_{VMC} = 2.5$ V	–	4	10	$\mu$ A
		power-down; PDx = 01; $V_{VMC} = 2.5$ V; SCL = 1; SDA = 1	–	4	10	$\mu$ A
		standby; PDx = 11; $V_{VMC} = 2.5$ V; SCL = 1; SDA = 1	–	2	5	$\mu$ A
$V_P$ : SUPPLY OUTPUT FOR ELECTRET MICROPHONE						
$V_P$	output voltage	$I_{VP} = 500$ $\mu$ A	1.6	1.9	–	V
$Z_{VP}$	output impedance	f = 300 Hz	–	40	–	$\Omega$
$PSR_{VP}$	power supply rejection	f = 300 Hz; note 5	–	65	–	dB
<b>Reset functions: <math>V_{DD}</math>, <math>V_{MC}</math> and RMC</b>						
INTERNAL RESET						
$V_{DD(sw)}$	switching level of $V_{DD}$ below which internal reset is active	$T_{amb} = -10$ to $+60$ °C; note 6	1.0	1.2	1.4	V
RMC: RESET OUTPUT FOR MICROCONTROLLER						
$V_{VMC(sw)}$	voltage level at pin VMC where RMC changes state	note 7	1.8	2.0	2.2	V
		power-down; PDx = 01; note 7	1.8	2.0	2.2	V
		standby; PDx = 11; note 7	1.8	2.1	2.4	V
$\Delta V_{VMC}/\Delta T$	voltage variation with ambient temperature	$T_{amb} = -10$ to $+60$ °C	–	0	–	mV/°C
		power-down; PDx = 01; $T_{amb} = -10$ to $+60$ °C	–	0	–	mV/°C
		standby; PDx = 11; $T_{amb} = -10$ to $+60$ °C	–	+3	–	mV/°C

# Multistandard programmable analog CMOS transmission IC

PCA1070

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Sending channel: MIC+, MIC-, DTMF, OMIC, LN, SCR, REG and LSI</b>						
<b>MIC+ AND MIC-: MICROPHONE INPUTS</b>						
Z <sub>MIC</sub>	input impedance	differential	60	100	–	kΩ
		single-ended	30	50	–	kΩ
CMRR <sub>MIC</sub>	common mode rejection ratio	note 8	–	72	–	dB
V <sub>MIC(peak)</sub>	allowed input signal voltage level (peak value)		–	–	70	mV
G <sub>M</sub>	gain MIC+/MIC- to LN		39.5	41	42.5	dB
G <sub>M(min)</sub>	minimum selectable gain	GMAx = 000100	28.5	30	31.5	dB
G <sub>M(max)</sub>	maximum selectable gain	GMAx = 011001	49.5	51	52.5	dB
G <sub>M(step)</sub>	step resolution		–	1	–	dB
ΔG <sub>M</sub>	gain variation with frequency	at f = 300 Hz and 3400 Hz with respect to 1 kHz; note 9	–	–	+0.3/–0.7	dB
	gain variation with ambient temperature	at T <sub>amb</sub> = –10 to +60 °C with respect to 25 °C	–	±0.2	–	dB
	gain variation with line current	at I <sub>line</sub> = 100 mA with respect to 20 mA; note 9	–	0	±0.5	dB
t <sub>ACM</sub>	AC start-up time	C <sub>VDD</sub> = 470 μF; note 10	–	150	–	ms
<b>Sending mute/privacy switch</b>						
ΔG <sub>M</sub>	reduction of G <sub>M</sub>	SM = 1	–	100	–	dB
<b>DTMF: DUAL TONE MULTI-FREQUENCY INPUT</b>						
R <sub>DTMF</sub>	parallel input resistance	SM = 1	100	200	–	kΩ
C <sub>DTMF</sub>	parallel input capacitance	SM = 1	–	45	–	pF
G <sub>DTMF</sub>	gain from DTMF to LN	SM = 1	20	21	22	dB
G <sub>DTMF(min)</sub>	minimum selectable gain	SM = 1; GMAx = 100101	0	1	2	dB
G <sub>DTMF(max)</sub>	maximum selectable gain	SM = 1; GMAx = 001111	20	21	22	dB
G <sub>DTMF(step)</sub>	step resolution	SM = 1	–	1	–	dB
ΔG <sub>DTMF</sub>	gain variation with frequency	SM = 1; at f = 300 Hz and 3400 Hz with respect to 1 kHz; note 9	–	–	+0.3/–0.7	dB
	gain variation with ambient temperature	SM = 1; at T <sub>amb</sub> = –10 to +60 °C with respect to 25 °C	–	±0.2	–	dB
	gain variation with line current	SM = 1; at I <sub>line</sub> = 100 mA with respect to 20 mA; note 9	–	0	±0.5	dB
<b>Confidence tone</b>						
G <sub>CTS</sub>	gain from DTMF to QR+/QR-;	RM = 1; SM = 1; notes 11 and 12	–	–25	–	dB
G <sub>CTS(min)</sub>	minimum selectable gain	RM = 1; SM = 1; GRAx = 111001	–	–40	–	dB
G <sub>CTS(max)</sub>	maximum selectable gain	RM = 1; SM = 1; GRAx = 100000	–	–19	–	dB
G <sub>CTS(step)</sub>	step resolution	RM = 1; SM = 1	–	0.5 to 1	–	dB

# Multistandard programmable analog CMOS transmission IC

PCA1070

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>OMIC: MICROPHONE PREAMPLIFIER OUTPUT</b>						
Z <sub>OMIC</sub>	output impedance		–	400	–	Ω
G <sub>OMIC</sub>	gain from MIC+/MIC– to OMIC	dynamic limiter not active; note 13	–	20	–	dB
<b>LN: SENDING CHANNEL OUTPUT; notes 14 and 15</b>						
BRL	balance return loss Z <sub>LN</sub> with Z <sub>ref</sub> = 220 Ω + (820 Ω // 115 nF)	Z <sub>line</sub> = ∞ Ω; f = 300 Hz	20	37	–	dB
		Z <sub>line</sub> = ∞ Ω; f = 1 kHz	20	35	–	dB
		Z <sub>line</sub> = ∞ Ω; f = 3.4 kHz	20	25	–	dB
<i>Selectable values for Z<sub>set</sub> = R<sub>a</sub> + (R<sub>b</sub> // C) with C = 1/(2π × R<sub>b</sub> × f<sub>p</sub>); note 16</i>						
R <sub>a</sub>	non-shunted resistance of Z <sub>set</sub>		–	200	–	Ω
R <sub>a(min)</sub>	minimum selectable value for R <sub>a</sub>	ZSAX = 001; note 17	–	0	–	Ω
R <sub>a(max)</sub>	maximum selectable value for R <sub>a</sub>	ZSAX = 11x	–	600	–	Ω
R <sub>a(step)</sub>	step resolution for R <sub>a</sub>		–	100	–	Ω
R <sub>b</sub>	shunted resistance of Z <sub>set</sub>		–	800	–	Ω
R <sub>b(min)</sub>	minimum selectable value for R <sub>b</sub>	ZSBx = 001; notes 17 and 18	–	600	–	Ω
R <sub>b(max)</sub>	maximum selectable value for R <sub>b</sub>	ZSBx = 1x1	–	1000	–	Ω
R <sub>b(step)</sub>	step resolution for R <sub>b</sub>		–	100	–	Ω
f <sub>p</sub>	pole frequency determining shunt capacitance C		–	1915	–	Hz
f <sub>p(min)</sub>	minimum selectable f <sub>p</sub>	ZSPx = 0000	–	828	–	Hz
f <sub>p(max)</sub>	maximum selectable f <sub>p</sub>	ZSPx = 0111; note 19	–	5859	–	Hz
n	multiplication factor for f <sub>p</sub>	f <sub>p</sub> (x + 1) = n × [f <sub>p</sub> (x)]	–	1.322	–	
V <sub>LN(noise)</sub>	noise output voltage	psophometrically weighted (O41 curve)	–	–76	–	dBmp
<b>Dynamic limiter</b>						
V <sub>LN(p-p)</sub>	threshold of dynamic limiter (peak-to-peak)		3.1	3.5	3.9	V
		DLT = 1	2.2	2.6	3.0	V
		low voltage condition; V <sub>SLPE</sub> = 3.1 V	–	2.4	–	V
		low current condition; I <sub>line</sub> = 9 mA	–	2.6	–	V
THD	total harmonic distortion	V <sub>i</sub> = 12 mV (RMS) + 10 dB	–	2.5	5.0	%
<b>Dynamic behaviour of limiter; note 20</b>						
t <sub>att</sub>	attack time	V <sub>i</sub> steps from 12 to 38 mV (RMS)	–	1.5	–	ms
t <sub>rel</sub>	release time	V <sub>i</sub> steps from 38 to 12 mV (RMS)	–	90	–	ms

# Multistandard programmable analog CMOS transmission IC

PCA1070

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SCR: PIN FOR SENDING CURRENT RESISTOR						
V <sub>SCR</sub>	voltage at pin SCR		–	0.28	–	V
		reduced sending gain; G <sub>M</sub> = 30 dB; G <sub>MAx</sub> = 000100	–	0.26	–	V
		I <sub>line</sub> = 12 mA	–	0.22	–	V
		I <sub>line</sub> = 7 mA	–	0.13	–	V
<b>Receiving channel: LN, LSI, OREC, QR+ and QR–</b>						
QR+, QR–: RECEIVING AMPLIFIER OUTPUTS						
Z <sub>QR+</sub> , Z <sub>QR–</sub>	output impedance	single-ended	–	4	–	Ω
G <sub>RS</sub>	gain from LN to QR+/QR–	note 21	–7.5	–6	–4.5	dB
G <sub>RS(min)</sub>	minimum selectable gain	GR <sub>Ax</sub> = 110011	–20.5	–19	–17.5	dB
G <sub>RS(max)</sub>	maximum selectable gain	GR <sub>Ax</sub> = 001011	9.5	11.0	12.5	dB
G <sub>RS(step)</sub>	gain step resolution		–	1	–	dB
ΔG <sub>RS</sub>	gain variation with frequency	at f = 300 Hz and 3400 Hz with respect to 1 kHz; note 9	–	–	±0.5	dB
ΔG <sub>RS</sub>	gain variation with temperature	at T <sub>amb</sub> = –10 to +60 °C with respect to 25 °C	–	±0.2	–	dB
ΔG <sub>RS</sub>	gain variation with line current	at I <sub>line</sub> = 100 mA with respect to 20 mA; note 9	–	0	±0.5	dB
t <sub>ACR</sub>	AC start-up time	C <sub>VDD</sub> = 470 μF; note 10	–	140	–	ms
V <sub>QR(p-p)</sub>	maximum output voltage swing (peak-to-peak)	V <sub>DD</sub> = 5 V; GR <sub>Ax</sub> = 001011; R <sub>t</sub> = ∞ Ω; RFC = 1; V <sub>LN</sub> = 2 V (RMS)	–	2.3	–	V
		HPL = 1; V <sub>DD</sub> = 5 V; GR <sub>Ax</sub> = 001011; R <sub>t</sub> = ∞ Ω; RFC = 1; V <sub>LN</sub> = 2 V (RMS)	–	5.9	–	V
V <sub>QR(rms)</sub>	output voltage (RMS value); THD = 2%	HPL = 1; GR <sub>Ax</sub> = 000011; note 22	0.45	–	–	V
		HPL = 1; R <sub>t</sub> = 450 Ω; GR <sub>Ax</sub> = 000011; note 22	0.84	–	–	V
		RFC = 1; C <sub>t</sub> = 80 nF; f = 3.4 kHz; GR <sub>Ax</sub> = 000011; note 22	0.9	–	–	V
		single-ended; HPL = 1; Z <sub>t</sub> = 150 Ω + 100 μF at QR–; GR <sub>Ax</sub> = 001001; note 22	0.45	–	–	V
V <sub>QR(noise)</sub>	noise output voltage	psophometrically weighted (O41 curve)	–	–82	–	dBmp
V <sub>QR(offset)</sub>	DC offset voltage between QR+/QR–		–	–	±100	mV
OREC: OUTPUT RECEIVE PREAMPLIFIER						
Z <sub>OREC</sub>	output impedance		–	1 000	–	Ω
G <sub>OREC</sub>	gain from LN to OREC	note 13	–	–6	–	dB

# Multistandard programmable analog CMOS transmission IC

PCA1070

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<i>Selectable values for <math>Z_{oss} = R_{sa} (R_{sb} // C_s)</math>; note 23</i>						
$R_{sa}$	non-shunted resistance of $Z_{oss}$		–	492	–	$\Omega$
$R_{sa(min)}$	minimum selectable value $R_{sa}$	ZOSA <sub>x</sub> = 0000	–	134	–	$\Omega$
$R_{sa(max)}$	maximum selectable value for $R_{sa}$	ZOSA <sub>x</sub> = 1010; note 24	–	492	–	$\Omega$
$R_{sb}$	shunted resistance of $Z_{oss}$		–	1259	–	$\Omega$
$R_{sb(min)}$	minimum selectable value for $R_{sb}$	ZOSB <sub>x</sub> = 0000	–	465	–	$\Omega$
$R_{sb(max)}$	maximum selectable value for $R_{sb}$	ZOSB <sub>x</sub> = 1011; note 24	–	2216	–	$\Omega$
$C_s$	shunt capacitance of $Z_{oss}$		–	134	–	nF
$C_{s(min)}$	minimum selectable value for $C_s$	ZOSP <sub>x</sub> = 0001; note 25	–	55	–	nF
$C_{s(max)}$	maximum selectable value for $C_s$	ZOSP <sub>x</sub> = 1111; note 24	–	259	–	nF
<i>Sidetone suppression; note 26</i>						
$G_{STS}$	gain from MIC+/MIC– to QR+/QR–	$Z_{line} = 492 \Omega + (1259 \Omega // 134 \text{ nF})$ ; $f = 300 \text{ Hz}$	–	11	15	dB
		$Z_{line} = 492 \Omega + (1259 \Omega // 134 \text{ nF})$ ; $f = 1 \text{ kHz}$	–	5	10	dB
		$Z_{line} = 492 \Omega + (1259 \Omega // 134 \text{ nF})$ ; $f = 3.4 \text{ kHz}$	–	9	15	dB
<b>Dial output connection: DOC (open-drain output)</b>						
$I_{DOC}$	output sink current	$V_{DOC} = 12 \text{ V}$	–	0	100	nA
		DPI = 1; $V_{DOC} = 0.4 \text{ V}$ ; $V_{DD} = 2.5 \text{ V}$	200	400	–	$\mu\text{A}$
<b>Line current control: LN and SLPE</b>						
$I_{line(min)}$	minimum value of DC line current that can be read as a bit code via the I <sup>2</sup> C-bus	LC <sub>x</sub> = 00001	–	15	–	mA
$I_{line(max)}$	maximum value of DC line current that can be read as a bit code via the I <sup>2</sup> C-bus	LC <sub>x</sub> = 11110	–	91	–	mA
$I_{line(step)}$	DC line current step resolution	note 27	–	≈2.5	–	mA
<b>I<sup>2</sup>C-bus inputs/outputs: SDA and SCL</b>						
	in accordance with standard	note 28	–	–	–	



# Multistandard programmable analog CMOS transmission IC

PCA1070

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Clock input: CLK</b>						
$V_{\text{CLK(p-p)}}$	input signal voltage level (peak-to-peak value)		200	–	$V_{\text{VMC}} - V_{\text{SS}}$	mV
$\Delta f_{\text{CLK}}/f_{\text{CLK}}$	frequency tolerance	note 29	–	–	$\pm 0.5$	%
$R_{\text{CLK}}$	input series resistance		–	800	–	$\text{k}\Omega$
$C_{\text{CLK}}$	input series capacitance		–	4	–	pF

## Notes

- Time needed to reach at start-up the default DC voltage  $V_{\text{SLPE}}$  ( $\pm 10\%$  from its final value):
  - Time depends strongly on the value of the capacitor(s) at  $V_{\text{DD}}$  and  $V_{\text{MC}}$ ; with a lower value of  $C_{\text{VDD}}$  the DC start-up time decreases.
  - The start-up time can be reduced considerably by programming the bit code  $\text{DST} = 1$  during the start-up procedure. In practice this is possible as soon as the microcontroller has become operational.
- Time needed to reach the DC voltage  $V_{\text{SLPE}}$  within  $\pm 10\%$  from its final value) after reprogramming VDCx.
- The supply voltage  $V_{\text{DD}}$  is determined by the regulated DC voltage at pin SLPE and by the voltage drop between pin SLPE and  $V_{\text{DD}}$ ; see Chapter “Functional description”.
- Relaxed performance means: parameters can deviate from their specified values.
- Rejection between supply pin  $V_{\text{DD}}$  and  $V_{\text{P}}$ . Rejection between pin LN and  $V_{\text{P}}$  can be calculated by adding the attenuation of the first-order low-pass filter ( $R = 250 \Omega$ ,  $C = 150 \mu\text{F}$ ) between SLPE and  $V_{\text{DD}}$ .
- If  $V_{\text{DD}}$  is above this level, the default values have been loaded into the internal registers.
- RMC changes from logic 1 to logic 0 when voltage on pin VMC is increasing; RMC changes from logic 0 to logic 1 when voltage on pin VMC is decreasing; see Fig.4.
- Common mode signal is applied via  $2 \times 470 \Omega$  external resistors connected to pins MIC+ and MIC–.
- Not tested, guaranteed by design.
- Time needed to reach default settings ( $\pm 3 \text{ dB}$ ).
- At low gain settings the confidence tone gain will be slightly higher than the specified value due to a residual signal.
- $G_{\text{CTA}}$ , the confidence tone gain for asymmetrical drive, equals  $G_{\text{CTS}} - 6$  (in dB).
- To be left open-circuit in application.
- The AC set impedance between pin LN and  $V_{\text{SS}}$  consists of  $R_{\text{a}} + (R_{\text{b}} // C)$  in parallel with an artificial inductor  $L_{\text{eq}}$  and internal resistors  $R_{\text{p}}$  and  $R_{\text{LSI}}$  and internal capacitor  $C_{\text{p}}$ . See Chapter “Functional description”.
- Balance Return Loss indicates the deviation of an impedance with respect to a reference impedance.  
 $\text{BRL} = 20 \log |(Z_{\text{LN}} + Z_{\text{ref}})/(Z_{\text{LN}} - Z_{\text{ref}})|$  where  $Z_{\text{LN}} \approx R_{\text{a}} + (R_{\text{b}} // C)$  is the impedance seen into pin LN  
 $Z_{\text{ref}} = R_{\text{a(ref)}} + (R_{\text{b(ref)}} // C_{\text{ref}})$  is the reference impedance.
- Without clock the set impedance is automatically set to  $Z_{\text{set}} = 600 \Omega$  (typical).
- The combination  $R_{\text{a}} = 0$  and  $R_{\text{b}} = 0$  is not allowed (see Tables 9 and 10, note 1).
- Value logic 0 can also be programmed.
- Value  $f_{\text{p}} = 12 \text{ kHz}$  can also be programmed.
- Attack and release times are also valid under low current and voltage conditions.
- $G_{\text{RA}}$ , the receiving channel gain for asymmetrical drive equals  $G_{\text{RS}} - 6$  (in dB).
- The maximum possible output swing depends on the DC conditions (the programmed voltage  $V_{\text{SLPE}}$  and the load on the supply pin  $V_{\text{DD}}$ ) and on the gain setting of the receiving channel.

---

**Multistandard programmable analog  
CMOS transmission IC**

---

**PCA1070**

23. The internal balance impedance  $Z_{oss}$  to match the external load impedance at pin LN ( $Z_{line} = Z_{oss}$ ) for optimum sidetone suppression;  $Z_{oss} = R_{sa} + (R_{sb} // C_s)$ ; without clock the sidetone balance impedance is automatically set to  $Z_{oss} = 600 \Omega$  (typical).
24. Other values can be found in Tables 14, 15 and 16.
25. Value  $C_s = 5 \text{ nF}$  can also be programmed.
26. Gain sending channel  $G_M = \text{default}$  (typical 41 dB); gain receiving channel  $G_{rec} = \text{default}$  (typical -6 dB); sidetone gain  $G_{STS}$  minimum sidetone suppression at  $f = 300 \text{ Hz}$  and  $3400 \text{ Hz}$  is:  $G_M + G_R - G_{st(max)} = 41 - 6 - 15 = 20 \text{ dB}$ .  $G_{STA}$ , the sidetone gain for asymmetrical drive equals  $G_{STS} - 6$  (in dB).
27. Indication only; exact values can be found in Table 16.
28. Standard I<sup>2</sup>C-bus specifications are valid for  $V_{DD} \geq 2.5 \text{ V}$ . Relaxed specifications for  $V_{DD} = 1.8$  to  $2.5 \text{ V}$ .
29. Recommended accuracy of input frequency; a higher tolerance will cause parameters to deviate from their specified values; note that all parameters are specified with the reference input clock frequency  $f_{clk} = 3.579545 \text{ MHz}$ .

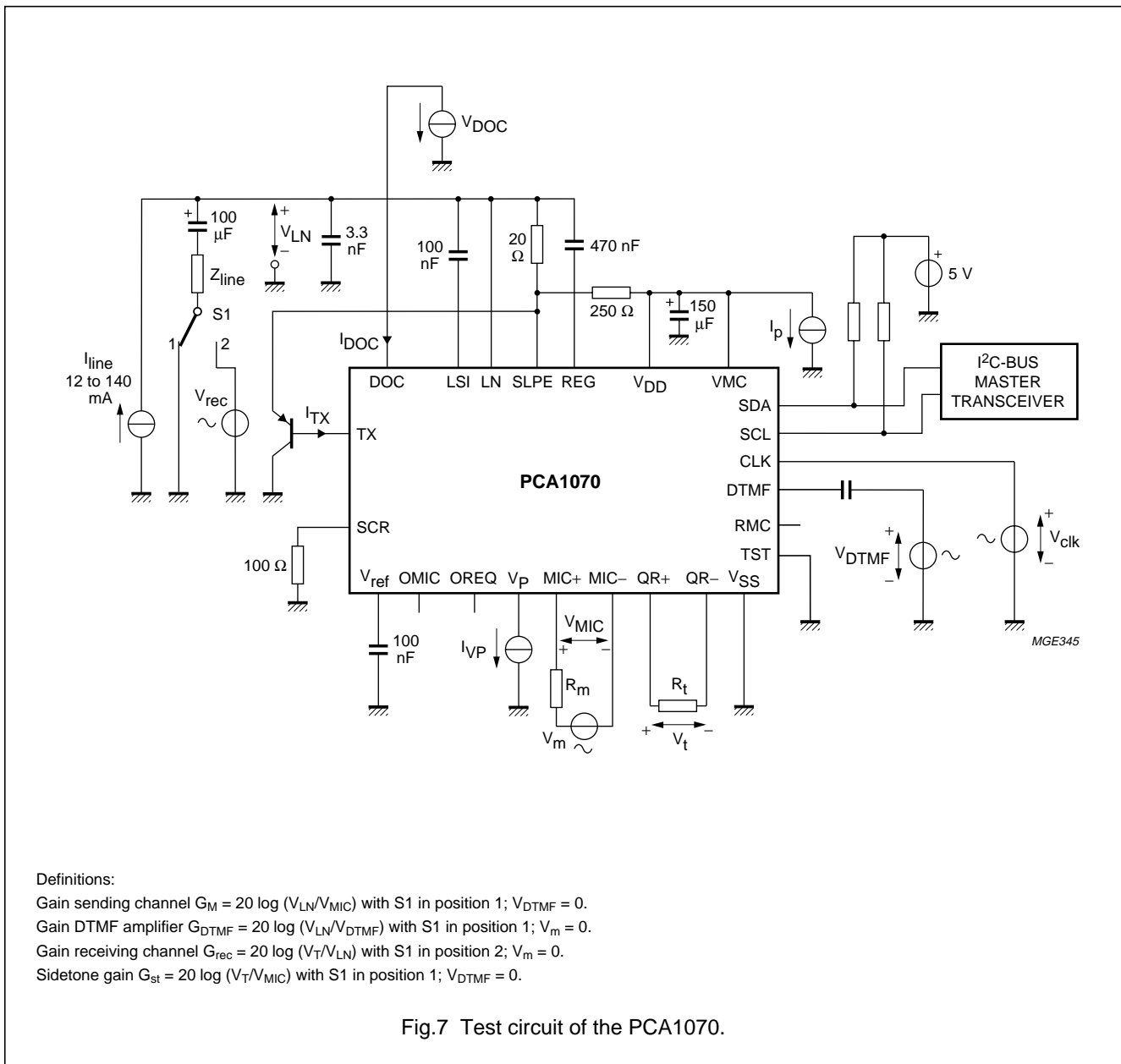
# Multistandard programmable analog CMOS transmission IC

PCA1070

## TEST AND APPLICATION INFORMATION

The test circuit is illustrated in Fig.7. The basic application circuit is illustrated in Fig.8. An interrupter with an N-channel depletion MOS transistor (e.g. BSD254A or BSP124) is shown. It is intended for applications where a low DC line voltage is required. An interrupter with an N-channel enhancement MOS transistor (e.g. BSN304A or BSP130) can be used for applications where a relatively high DC line voltage is allowed.

An application circuit for applications where a low DC line voltage and long line interrupts are required, is illustrated in Fig.9 (interrupter with an N-channel depletion MOS transistor).



# Multistandard programmable analog CMOS transmission IC

PCA1070

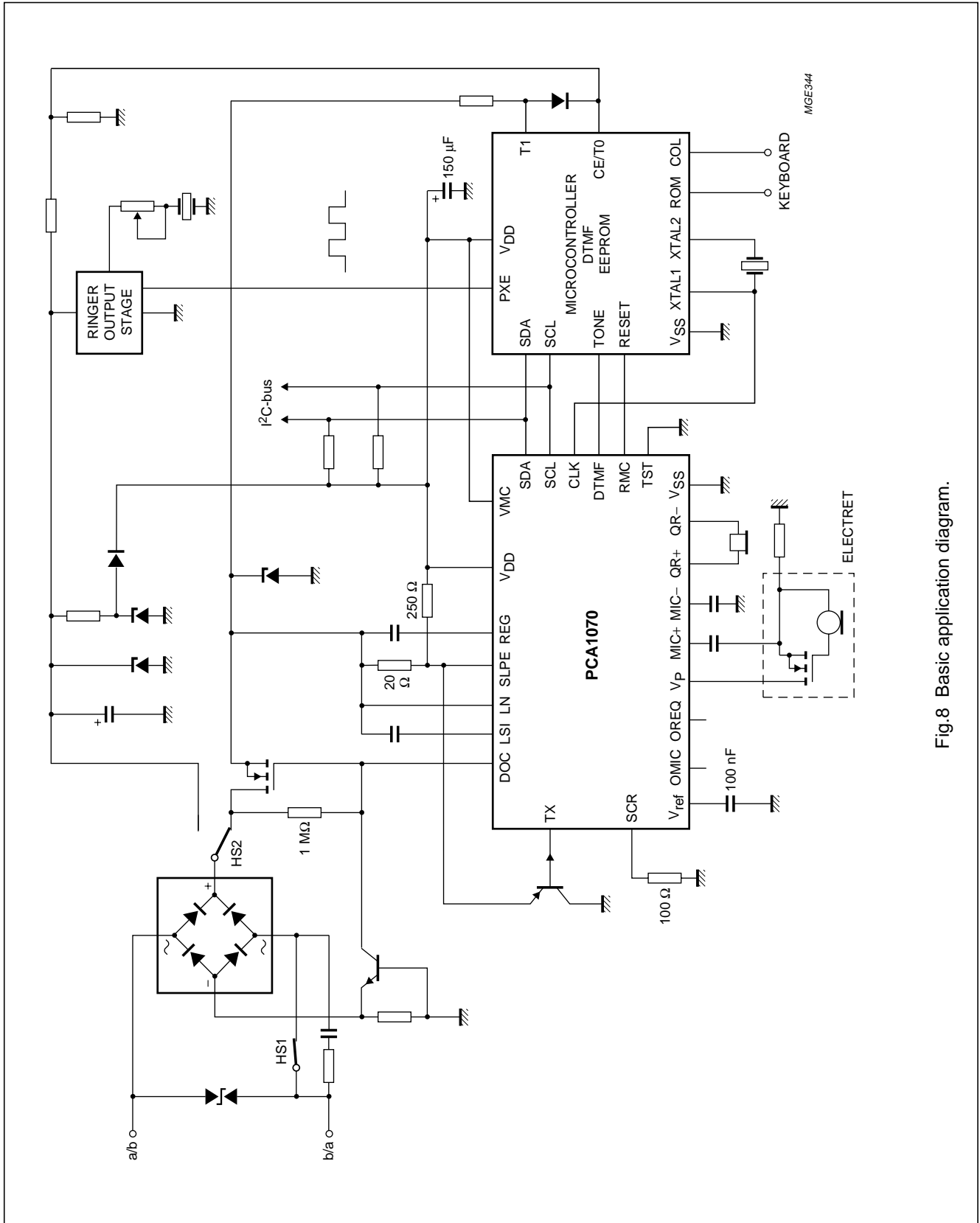


Fig.8 Basic application diagram.

# Multistandard programmable analog CMOS transmission IC

PCA1070

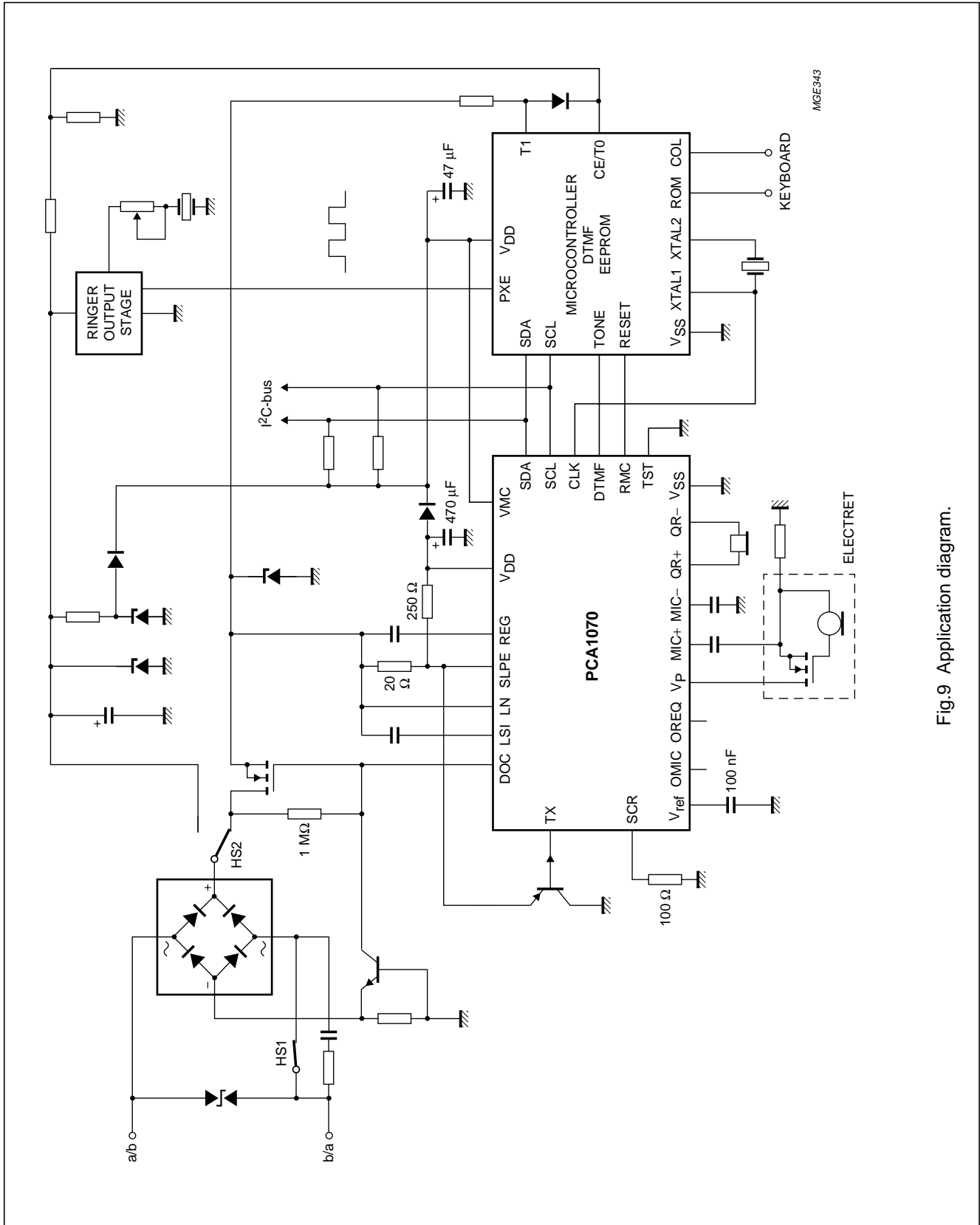


Fig.9 Application diagram.

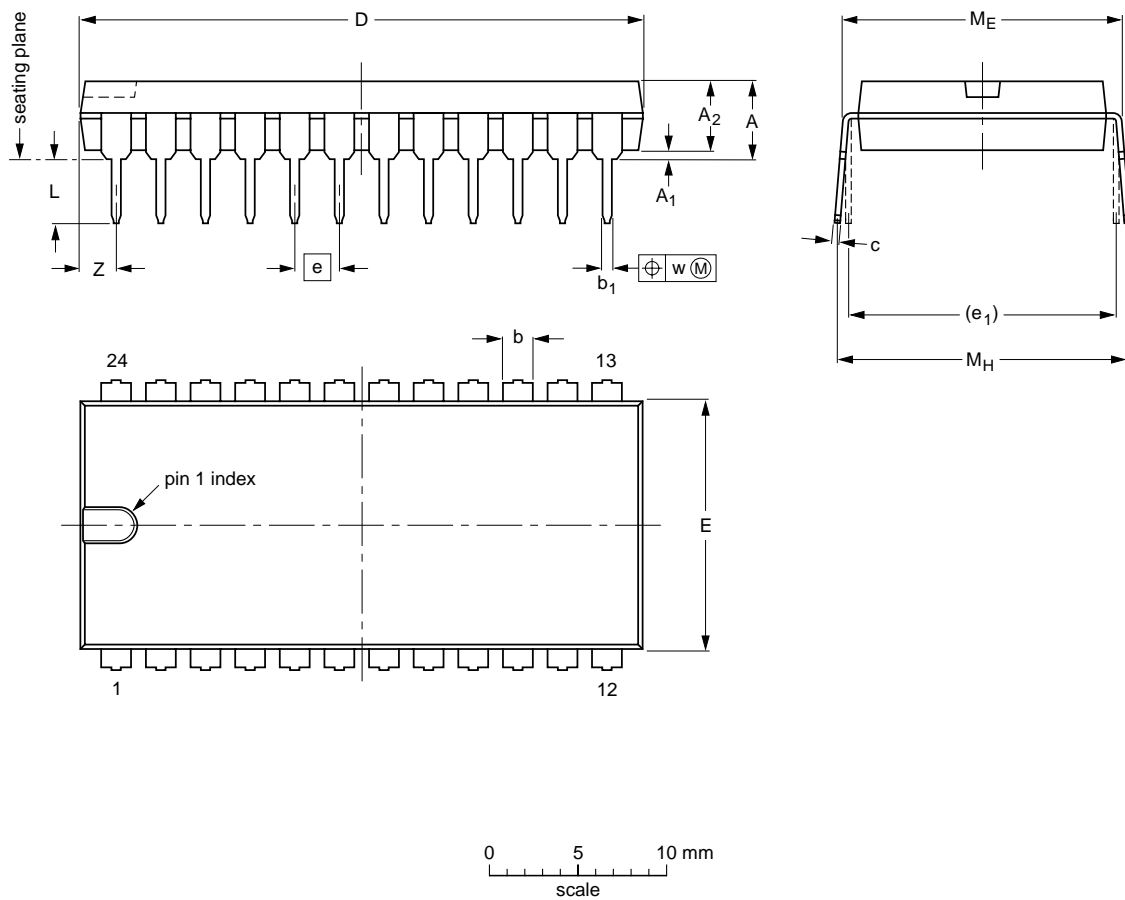
Multistandard programmable analog  
CMOS transmission IC

PCA1070

PACKAGE OUTLINES

DIP24: plastic dual in-line package; 24 leads (600 mil)

SOT101-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>1</sub>	L	M <sub>E</sub>	M <sub>H</sub>	w	Z <sup>(1)</sup> max.
mm	5.1	0.51	4.0	1.7 1.3	0.53 0.38	0.32 0.23	32.0 31.4	14.1 13.7	2.54	15.24	3.9 3.4	15.80 15.24	17.15 15.90	0.25	2.2
inches	0.20	0.020	0.16	0.066 0.051	0.021 0.015	0.013 0.009	1.26 1.24	0.56 0.54	0.10	0.60	0.15 0.13	0.62 0.60	0.68 0.63	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

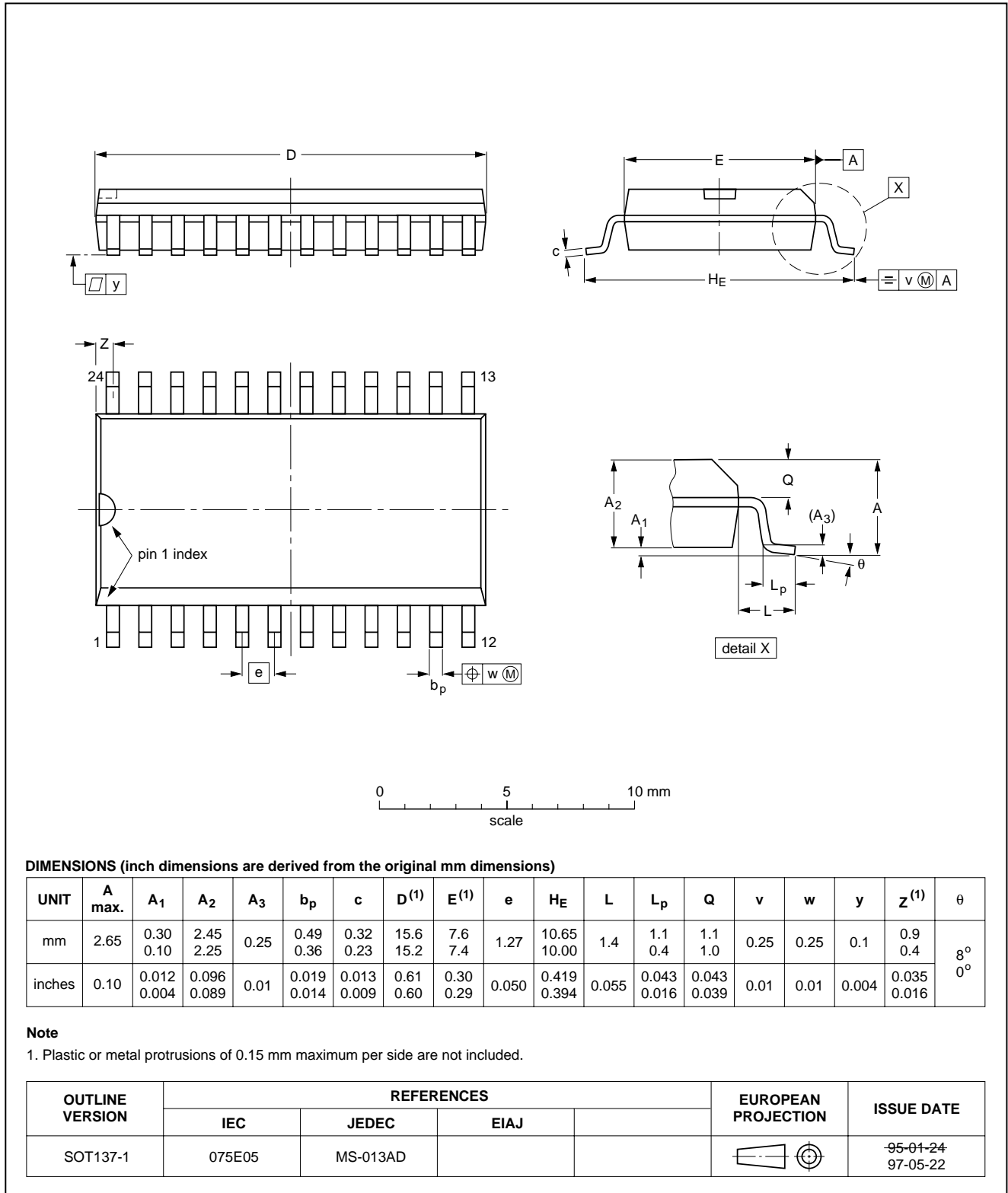
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT101-1	051G02	MO-015AD				92-11-17 95-01-23

Multistandard programmable analog  
CMOS transmission IC

PCA1070

SO24: plastic small outline package; 24 leads; body width 7.5 mm

SOT137-1



## Multistandard programmable analog CMOS transmission IC

PCA1070

### SOLDERING

#### Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

#### DIP

##### SOLDERING BY DIPPING OR BY WAVE

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ( $T_{stg\ max}$ ). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

##### REPAIRING SOLDERED JOINTS

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

#### SO

##### REFLOW SOLDERING

Reflow soldering techniques are suitable for all SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

##### WAVE SOLDERING

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used
- The longitudinal axis of the package footprint must be parallel to the solder flow
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

##### REPAIRING SOLDERED JOINTS

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.



Multistandard programmable analog  
CMOS transmission IC

PCA1070

**DEFINITIONS**

<b>Data sheet status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Limiting values</b>	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	

**LIFE SUPPORT APPLICATIONS**

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

**PURCHASE OF PHILIPS I<sup>2</sup>C COMPONENTS**



Purchase of Philips I<sup>2</sup>C components conveys a license under the Philips' I<sup>2</sup>C patent to use the components in the I<sup>2</sup>C system provided the system conforms to the I<sup>2</sup>C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

---

Multistandard programmable analog  
CMOS transmission IC

---

PCA1070

**NOTES**

---

Multistandard programmable analog  
CMOS transmission IC

---

PCA1070

**NOTES**

# Philips Semiconductors – a worldwide company

**Argentina:** see South America

**Australia:** 34 Waterloo Road, NORTH RYDE, NSW 2113,  
Tel. +61 2 9805 4455, Fax. +61 2 9805 4466

**Austria:** Computerstr. 6, A-1101 WIEN, P.O. Box 213,  
Tel. +43 1 60 101, Fax. +43 1 60 101 1210

**Belarus:** Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,  
220050 MINSK, Tel. +375 172 200 733, Fax. +375 172 200 773

**Belgium:** see The Netherlands

**Brazil:** see South America

**Bulgaria:** Philips Bulgaria Ltd., Energoproject, 15th floor,  
51 James Bourchier Blvd., 1407 SOFIA,  
Tel. +359 2 689 211, Fax. +359 2 689 102

**Canada:** PHILIPS SEMICONDUCTORS/COMPONENTS,  
Tel. +1 800 234 7381

**China/Hong Kong:** 501 Hong Kong Industrial Technology Centre,  
72 Tat Chee Avenue, Kowloon Tong, HONG KONG,  
Tel. +852 2319 7888, Fax. +852 2319 7700

**Colombia:** see South America

**Czech Republic:** see Austria

**Denmark:** Prags Boulevard 80, PB 1919, DK-2300 COPENHAGEN S,  
Tel. +45 32 88 2636, Fax. +45 31 57 0044

**Finland:** Sinikalliontie 3, FIN-02630 ESPOO,  
Tel. +358 9 615800, Fax. +358 9 61580920

**France:** 4 Rue du Port-aux-Vins, BP317, 92156 SURESNES Cedex,  
Tel. +33 1 40 99 6161, Fax. +33 1 40 99 6427

**Germany:** Hammerbrookstraße 69, D-20097 HAMBURG,  
Tel. +49 40 23 53 60, Fax. +49 40 23 536 300

**Greece:** No. 15, 25th March Street, GR 17778 TAVROS/ATHENS,  
Tel. +30 1 4894 339/239, Fax. +30 1 4814 240

**Hungary:** see Austria

**India:** Philips INDIA Ltd, Shivsagar Estate, A Block, Dr. Annie Besant Rd.  
Worli, MUMBAI 400 018, Tel. +91 22 4938 541, Fax. +91 22 4938 722

**Indonesia:** see Singapore

**Ireland:** Newstead, Clonskeagh, DUBLIN 14,  
Tel. +353 1 7640 000, Fax. +353 1 7640 200

**Israel:** RAPAC Electronics, 7 Kehilat Saloniki St, PO Box 18053,  
TEL AVIV 61180, Tel. +972 3 645 0444, Fax. +972 3 649 1007

**Italy:** PHILIPS SEMICONDUCTORS, Piazza IV Novembre 3,  
20124 MILANO, Tel. +39 2 6752 2531, Fax. +39 2 6752 2557

**Japan:** Philips Bldg 13-37, Kohnan 2-chome, Minato-ku, TOKYO 108,  
Tel. +81 3 3740 5130, Fax. +81 3 3740 5077

**Korea:** Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL,  
Tel. +82 2 709 1412, Fax. +82 2 709 1415

**Malaysia:** No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR,  
Tel. +60 3 750 5214, Fax. +60 3 757 4880

**Mexico:** 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905,  
Tel. +9-5 800 234 7381

**Middle East:** see Italy

**Netherlands:** Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB,  
Tel. +31 40 27 82785, Fax. +31 40 27 88399

**New Zealand:** 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,  
Tel. +64 9 849 4160, Fax. +64 9 849 7811

**Norway:** Box 1, Manglerud 0612, OSLO,  
Tel. +47 22 74 8000, Fax. +47 22 74 8341

**Philippines:** Philips Semiconductors Philippines Inc.,  
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI,  
Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

**Poland:** Ul. Lukiska 10, PL 04-123 WARSZAWA,  
Tel. +48 22 612 2831, Fax. +48 22 612 2327

**Portugal:** see Spain

**Romania:** see Italy

**Russia:** Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW,  
Tel. +7 095 755 6918, Fax. +7 095 755 6919

**Singapore:** Lorong 1, Toa Payoh, SINGAPORE 1231,  
Tel. +65 350 2538, Fax. +65 251 6500

**Slovakia:** see Austria

**Slovenia:** see Italy

**South Africa:** S.A. PHILIPS Pty Ltd., 195-215 Main Road Martindale,  
2092 JOHANNESBURG, P.O. Box 7430 Johannesburg 2000,  
Tel. +27 11 470 5911, Fax. +27 11 470 5494

**South America:** Rua do Rocio 220, 5th floor, Suite 51,  
04552-903 São Paulo, SÃO PAULO - SP, Brazil,  
Tel. +55 11 821 2333, Fax. +55 11 829 1849

**Spain:** Balmes 22, 08007 BARCELONA,  
Tel. +34 3 301 6312, Fax. +34 3 301 4107

**Sweden:** Kottbygatan 7, Akalla, S-16485 STOCKHOLM,  
Tel. +46 8 632 2000, Fax. +46 8 632 2745

**Switzerland:** Allmendstrasse 140, CH-8027 ZÜRICH,  
Tel. +41 1 488 2686, Fax. +41 1 481 7730

**Taiwan:** Philips Semiconductors, 6F, No. 96, Chien Kuo N. Rd., Sec. 1,  
TAIPEI, Taiwan Tel. +886 2 2134 2865, Fax. +886 2 2134 2874

**Thailand:** PHILIPS ELECTRONICS (THAILAND) Ltd.,  
209/2 Sanpavuth-Bangna Road Prakanong, BANGKOK 10260,  
Tel. +66 2 745 4090, Fax. +66 2 398 0793

**Turkey:** Talatpasa Cad. No. 5, 80640 GÜLTEPE/ISTANBUL,  
Tel. +90 212 279 2770, Fax. +90 212 282 6707

**Ukraine:** PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7,  
252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

**United Kingdom:** Philips Semiconductors Ltd., 276 Bath Road, Hayes,  
MIDDLESEX UB3 5BX, Tel. +44 181 730 5000, Fax. +44 181 754 8421

**United States:** 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,  
Tel. +1 800 234 7381

**Uruguay:** see South America

**Vietnam:** see Singapore

**Yugoslavia:** PHILIPS, Trg N. Pasica 5/v, 11000 BEOGRAD,  
Tel. +381 11 625 344, Fax. +381 11 635 777

**For all other countries apply to:** Philips Semiconductors, Marketing & Sales Communications,  
Building BE-p, P.O. Box 218, 5600 MD EINDHOVEN, The Netherlands, Fax. +31 40 27 24825

**Internet:** <http://www.semiconductors.philips.com>

© Philips Electronics N.V. 1997

SCA54

All rights are reserved. Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner.

The information presented in this document does not form part of any quotation or contract, is believed to be accurate and reliable and may be changed without notice. No liability will be accepted by the publisher for any consequence of its use. Publication thereof does not convey nor imply any license under patent- or other industrial or intellectual property rights.

Printed in The Netherlands

417027/00/03/pp36

Date of release: 1997 Jun 20

Document order number: 9397 750 00949

*Let's make things better.*

**Philips  
Semiconductors**



**PHILIPS**