AP561-F

0.7-2.9 GHz 8W HBT Power Amplifier

Applications

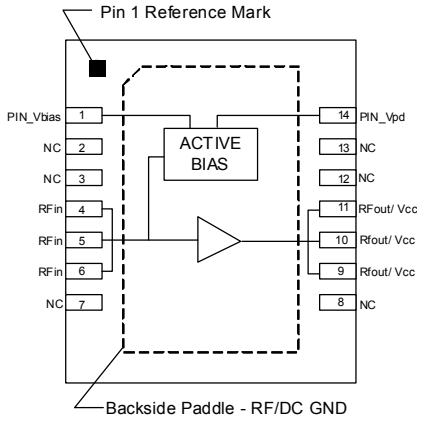
- Small Cells / Repeaters / DAS
- 3G / 4G Wireless Infrastructure
- Wireless Backhaul
- Portable Radios
- LTE / WCDMA / CDMA

14 Pin 5x6 mm DFN Package

Product Features

- 700-2900 MHz
- +39 dBm P1dB
- +12 V Supply Voltage
- -50 dBc ACLR @ 28dBm Pout
- 1.5% EVM @ 30 dBm Pout
- 13 dB Gain @ 2.6GHz
- Fast Shut-Down Capability
- Internal Active Bias and Temp Compensation
- Lead-free / RoHS-compliant

Functional Block Diagram



General Description

The AP561 is a high dynamic range broadband power amplifier in a surface mount package. The single-stage amplifier has 13 dB Gain, while being able to achieve high performance for 0.7–2.9 GHz applications with up to +39 dBm of compressed 1dB power.

The AP561 uses a high reliability +12V InGaP/GaAs HBT process technology. The device incorporates proprietary bias circuitry to compensate for variations in linearity and current draw over temperature. The device does not require any negative bias voltage; an internal active bias allows the AP561 to operate directly off a commonly used +12V supply and has the added feature of a +5V power down control pin. RoHS-compliant 5x6mm DFN package is surface mountable to allow for low manufacturing costs to the end user.

Pin Configuration

Pin No.	Label
1	PIN_V_{BIAS}
2, 3, 7, 8, 12, 13	N/C
4, 5, 6	RF IN
9, 10, 11	RF Output / V_{CC}
14	PIN_V_{PD}
Backside paddle	RF / DC GND

Ordering Information

Part No.	Description
AP561-F	0.7-2.9 GHz 12V 8W Power Amplifier
AP561-PCB900	869-894 MHz Evaluation Board
AP561-PCB2140	2110-2170 MHz Evaluation Board
AP561-PCB2500	2.5-2.7 GHz Evaluation Board

Standard T/R size = 1000 pieces on a 7” reel

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	−55 to 150°C
RF Input Power, CW, 50Ω, T=25°C	+33 dBm
Supply Voltage (V_{CC})	+15 V
BV_{cbo}	+35 V
Power Dissipation	14 W

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Supply Voltage (V_{CC})		12.0		V
T_{CASE}	−40		+85	°C
Tj for >10^6 hours MTTF			158	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Test conditions unless otherwise noted: V_{CC} =+12V, V_{PD} =+5V, Temp= +25°C, using AP561-PCB2600 application circuit

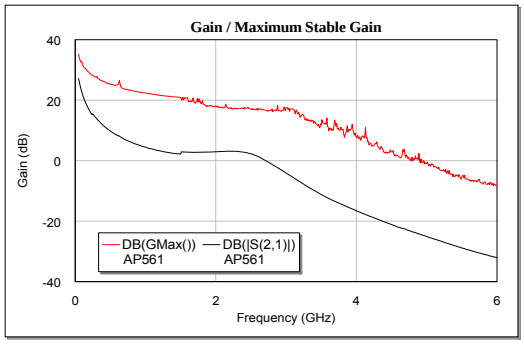
Parameter	Conditions	Min	Typ	Max	Units
Operational Frequency Range		700		2900	MHz
Test Frequency			2600		MHz
Output Channel Power			+30		dBm
Gain			13.0		dB
Input Return Loss			14.5		dB
Output Return Loss			6.5		dB
Error Vector Magnitude	See note 1.		1.7		%
Collector Efficiency			16.2		%
RF Switching Speed	See note 2.		50		ns
Output P1dB			+39		dBm
Operating Current, I_{CC}			510		mA
Quiescent Current, I_{CQ}			300		mA
Reference Current, I_{REF}			10		mA
Thermal Resistance, θ_{jc}	Module (junction to case)			6.0	°C/W

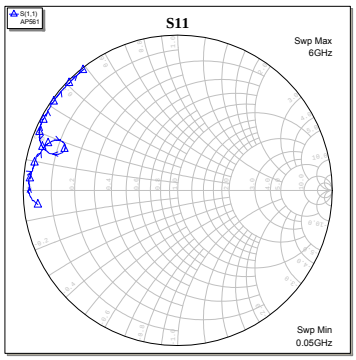
Notes:

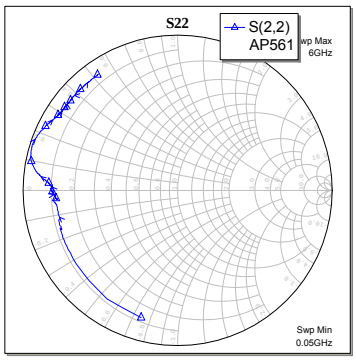
1. Using an 802.16-2004 OFDMA, 64QAM-1/2, 1024-FFT, 20 symbols, 30 subchannels signal, 9.5 dB PAR @ 0.01%.
2. Switching speed: 50% TTL to 100/0% RF. Vpd used for device power down (low=RF off).

Device Characterization

Test conditions unless otherwise noted: V_{CC} =+12V, V_{PD} =+5V, I_{CQ} = 300 mA (typ.), Temp= +25°C, calibrated to device pins







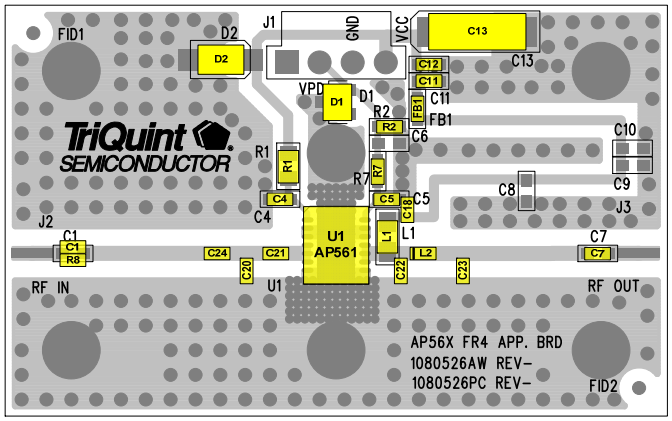
Notes:
The gain for the unmatched device in 50 ohm system is shown as the trace in black color. For a tuned circuit for a particular frequency, it is expected that actual gain will be higher, up to the maximum stable gain. The maximum stable gain is shown in red.

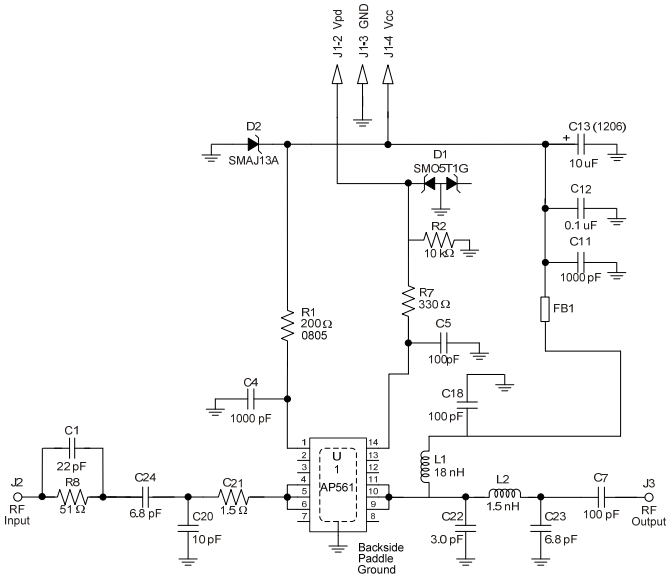
S-Parameters

Test conditions unless otherwise noted: V_{CC} =+12V, V_{PD} =+5V, Temp= +25°C, 50 Ohm system

Freq (GHz)	S11 (dB)	S11 (ang)	S21 (dB)	S21 (ang)	S12 (dB)	S12 (ang)	S22 (dB)	S22 (ang)
50	-0.83	-174.19	27.09	122.75	-43.35	29.12	-1.38	-106.01
100	-0.43	-177.42	22.26	106.35	-43.10	8.71	-1.82	-138.64
300	-0.35	179.26	14.06	89.18	-41.21	1.08	-2.02	-164.78
500	-0.32	177.35	9.81	79.93	-40.63	0.69	-2.10	-172.01
700	-0.34	175.28	7.08	71.64	-40.35	3.54	-2.09	-176.13
900	-0.40	173.11	5.19	63.88	-40.26	-3.79	-1.99	-177.89
1100	-0.47	170.97	3.82	55.72	-40.09	-9.55	-1.86	-178.93
1300	-0.53	168.26	2.80	47.12	-39.83	-16.44	-1.78	-179.77
1500	-0.59	165.56	2.18	37.92	-39.58	-23.59	-1.68	179.34
1700	-0.87	161.87	2.75	25.71	-38.56	-35.47	-1.67	177.40
1900	-1.14	158.99	2.84	12.58	-37.79	-49.59	-1.45	176.17
2100	-1.58	157.33	3.04	-4.10	-37.20	-69.96	-1.07	174.50
2300	-2.07	158.08	3.08	-26.45	-36.71	-98.60	-0.57	171.36
2500	-2.11	161.67	2.27	-53.16	-36.83	-134.34	-0.20	166.20
2700	-1.52	163.86	0.21	-79.14	-37.65	-170.26	-0.18	160.52
2900	-0.93	162.94	-2.57	-100.12	-38.71	157.51	-0.38	155.92
3100	-0.60	161.26	-5.57	-115.90	-39.66	133.27	-0.55	152.79
3300	-0.44	159.75	-8.55	-127.57	-40.18	115.97	-0.68	150.56
3500	-0.30	157.96	-11.15	-136.15	-40.26	102.36	-0.77	148.63
3700	-0.20	156.27	-13.44	-143.55	-40.26	94.11	-0.84	147.06
3900	-0.16	154.67	-15.57	-150.57	-39.83	85.11	-0.87	145.70
4100	-0.14	152.82	-17.53	-157.27	-39.91	78.44	-0.87	144.40
4300	-0.15	150.80	-19.35	-163.61	-39.49	72.37	-0.86	143.38
4500	-0.13	148.32	-21.11	-170.25	-39.09	66.71	-0.89	142.13

AP561-PCB900 Evaluation Board (896−894 MHz)





Notes:

1. See Evaluation Board PCB Information section for material and stack-up.
2. All components are of 0603 size unless stated on the schematic.
3. The right edge of C20 is placed at 153 mil from the AP561 RFin pin.
4. The right edge of C21 is placed at 55 mil from the AP561 RFin pin.
5. The right edge of C24 is placed at 230 mil from the AP561 RFin pin.
6. The left edge of C22 is placed at 78 mil from the AP561 RFout pin.
7. The left edge of L2 is placed at 135 mil from the AP561 RFout pin.
8. The left edge of C23 is placed at 265 mil from the AP561 RFout pin.
9. Do not exceed 5.5V on Vpd or damage to D1 will occur. Do not exceed 13V on Vcc or damage to D2 will occur.

Bill of Material – AP561-PCB900

Reference Des.	Value	Description	Manuf.	Part Number
N/A	N/A	Printed Circuit Board – FR4		
U1	N/A	0.7-2.9 GHz 8W Power Amplifier	TriQuint	AP561-F
C12	0.1 uF	CAP, 0603,10%, 50V, X7R	various	
C4, C11	1000 pF	CAP, 0603, 5%, 50V, NPO	various	
C5, C18, C7	100 pF	CAP, 0603, 5%, 50V, NPO	various	
C13	10 uF	CAP, 1206, 10%, 15V, Tantalum	various	
R1	200 Ω	RES, 0805, 5%, 1/10W. Chip.	various	
R7	330 Ω	RES, 0603,5%, 1/10W, Chip	various	
R2	10 kΩ	RES, 0603, 5%,1/16W, Chip	various	
R8	51 Ω	RES, 0603, 5%, 1/16W, Chip	various	
C1	22 pF	CAP, 0603, 5%, 50V, NPO/COG	various	
C20	10 pF	CAP, 0603, 2%, ACCU-P, 50V	AVX	06035J100GBSTR
C21	1.5 Ω	RES, 0603,5%, 1/10W, Chip	various	
C22	3.0 pF	CAP, 0603, ± 0.05pF, ACCU-P, 50V	AVX	06035J3R0ABSTR
C23, C24	6.8 pF	CAP, 0603, ± 0.05pF, ACCU-P, 50V	AVX	
L2	1.5 nH	IND, 0603, ±0.3nH	Toko	LL1608-FSL1N5S
L1	18 nH	IND, 0805, 5%, ceramic core	Coilcraft	0805HQ-18NXJC
FB1	N/A	Filter EMI Ferrite Bead	various	
D1	N/A	TVS Diode Array, 5V, SOT23, 2Ch	On-Semiconductor	SM05T1G
D2	N/A	Diode TVS, 13V, 400W, 5% SMA	On-Semiconductor	1SMA13AT3G

Typical Performance – AP561-PCB900

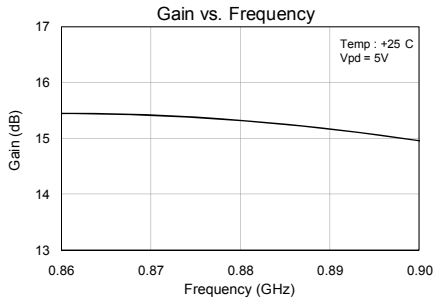
Test conditions unless otherwise noted: V_{CC} = +12 V, V_{PD} = +5 V, I_{CQ} = 300 mA (typ.), Temp=+25°C

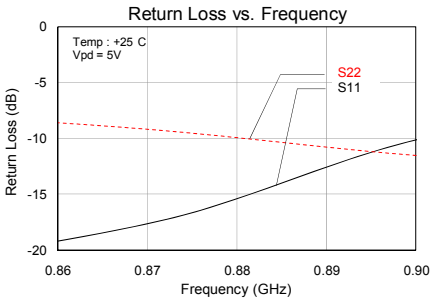
Parameter	Typical Values			Units
Frequency	869	880	894	MHz
Gain	15.4	15.2	15.0	dB
Input Return Loss	18	15	13	dB
Output Return Loss	9	10	11	dB
ACLR @ 29dBm Output Power [2]	-52	-52	-52	dBc
IMD3 @ 29dBm Output Power [1]	-46	-46.5	-47	dBc
Operating Current, I_{CC} @ 29dBm Output Power [2]	470	465	460	mA
Collector Efficiency @ 29dBm Output Power [2]	14	14.5	14.7	%
Output P1dB	39.2	39.1	38.9	dBm

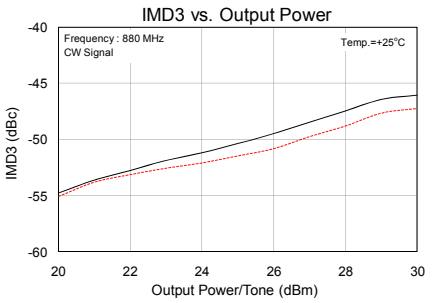
Notes:
1. IMD3 is measured with 1 MHz tone spacing.
2. ACLR test set-up: 3GPP WCDMA, TM1+64DPCH, +5MHz Offset, PAR = 10.2 dB @ 0.01% Probability.

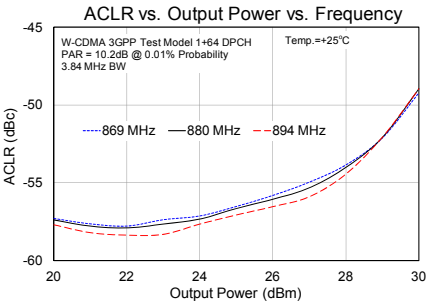
Performance Plots – AP561-PCB900

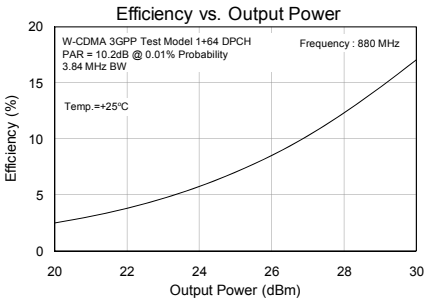
Test conditions unless otherwise noted: V_{CC} = +12 V, V_{PD} = +5 V, I_{CQ} = 300 mA (typ.), Temp=+25°C

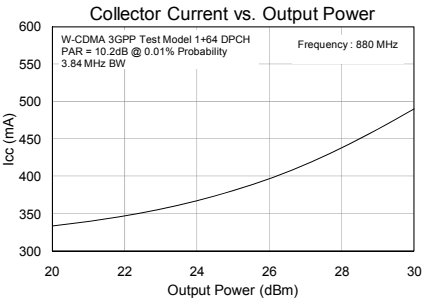




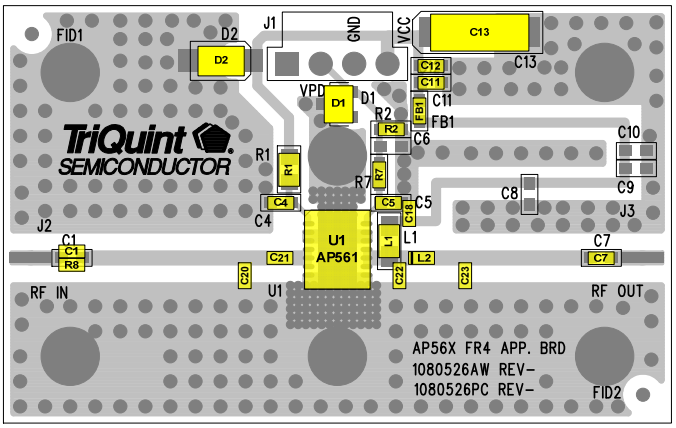


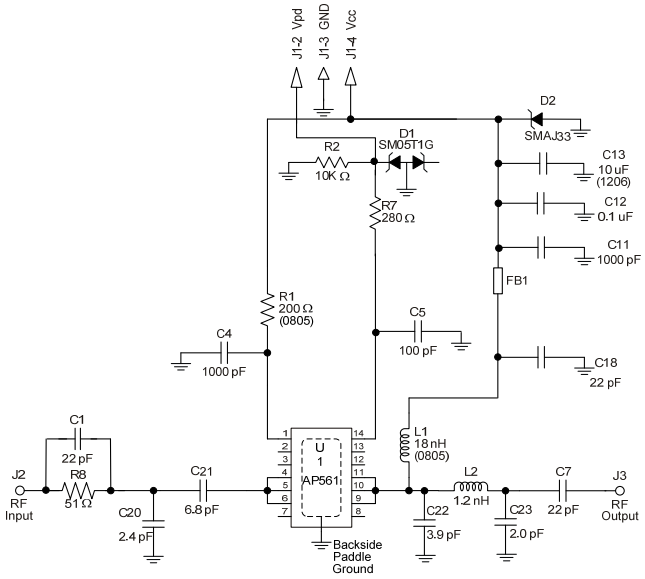






AP561-PCB2140 Evaluation Board (2110−2170 MHz)





Notes:

1. See Evaluation Board PCB Information section for material and stack-up.
2. All components are of 0603 size unless stated on the schematic.
3. The right edge of C20 is placed at 160 mil from the AP561 RFin pin.
4. The right edge of C21 is placed at 45 mil from the AP561 RFin pin.
5. The left edge of C22 is placed at 68 mil from the AP561 RFout pin.
6. The left edge of L2 is placed at 125 mil from the AP561 RFout pin.
7. The left edge of C23 is placed at 263 mil from the AP561 RFout pin.
8. Do not exceed 5.5V on Vpd or damage to D1 will occur. Do not exceed 13V on Vcc or damage to D2 will occur.
9. The primary RF microstrip line is 50Ω. The RF trace is cut at component C21 and L2 for this particular reference design.

Bill of Material – AP561-PCB2140

Reference Des.	Value	Description	Manuf.	Part Number
N/A	N/A	Printed Circuit Board – FR4		
U1	N/A	0.7-2.9 GHz 8W Power Amplifier	TriQuint	AP561-F
C12	0.1 uF	CAP, 0603,10%, 50V, X7R	various	
C4,C11	1000 pF	CAP, 0603, 5%, 50V, NPO	various	
C5	100 pF	CAP, 0603, 5%, 50V, NPO	various	
C13	10 uF	CAP, 1206, 10%, 15V, Tantalum	various	
R1	200 Ω	RES, 0805,5%,1/10W. CHIP.	various	
R7	280 Ω	RES, 0603,5%, 1/10W, Chip	various	
R2	10 kΩ	RES, 0603, 5%,1/16W, Chip	various	
C1, C7, C18	22 pF	CAP, 0603, 5%, 50V, NPO/COG	various	
C20	2.4 pF	CAP, 0603, ± 0.05 pF, ACCU-P, 50V	AVX	06035J2R4ABSTR
C21	6.8 pF	CAP, 0603, ± 0.1 pF, ACCU-P, 50V	AVX	06035J6R8ABSTR
C22	3.9 pF	CAP, 0603, ± 0.05pF, ACCU-P, 50V	AVX	06035J3R9ABSTR
C23	2.0 pF	CAP, 0603, ± 0.05pF, ACCU-P, 50V	AVX	06035J2R0ABSTR
L2	1.2 nH	IND, 0603, ±0.3nH	Toko	LL1608-FSL1N2S
L1	18 nH	IND, 0805, 5%, ceramic core	Coilcraft	0805HQ-18NXJC
FB1	N/A	Filter EMI Ferrite Bead	various	
D1	N/A	TVS Diode Array, 5V, SOT23, 2Ch	On-Semiconductor	SM05T1G
D2	N/A	Diode TVS, 13V, 400W, 5% SMA	On-Semiconductor	1SMA13AT3G

Typical Performance – AP561-PCB2140

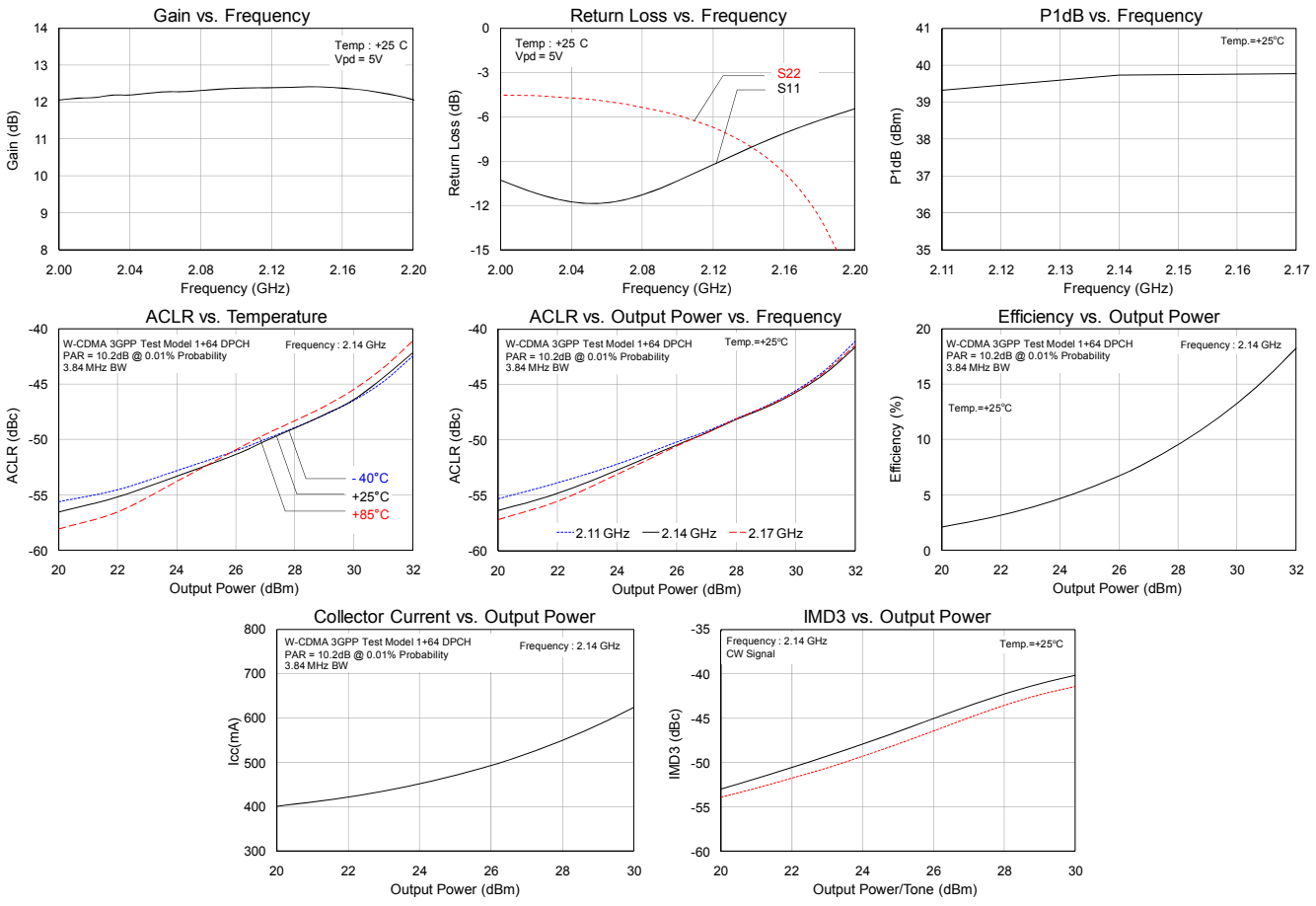
Test conditions unless otherwise noted: V_{CC} = +12 V, V_{PD} = +5 V, I_{CQ} = 370 mA (typ.), Temp=+25°C

Parameter	Typical Values			Units
Frequency	2110	2140	2170	MHz
Gain	12.4	12.4	12.3	dB
Input Return Loss	10	8	6.5	dB
Output Return Loss	6.3	8	11	dB
ACLR @ 28dBm Output Power [2]	-48	-48	-48	dBc
IMD3 @ 28dBm Output Power [1]	-42.7	-42.3	-43.8	dBc
Operating Current, I_{CC} @ 28dBm Output Power [2]	565	550	525	mA
Collector Efficiency @ 28dBm Output Power [2]	9	9.5	10	%
Output P1dB	39.3	39.7	39.7	dBm

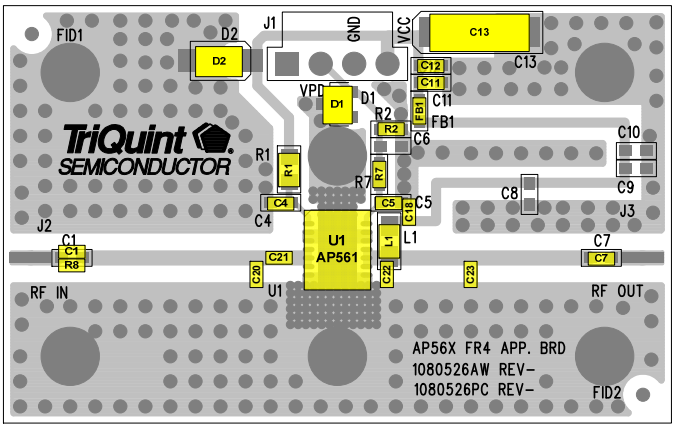
Notes:
1. IMD3 is measured with 1 MHz tone spacing.
2. ACLR test set-up: 3GPP WCDMA, TM1+64DPCH, +5MHz Offset, PAR = 10.2 dB @ 0.01% Probability.

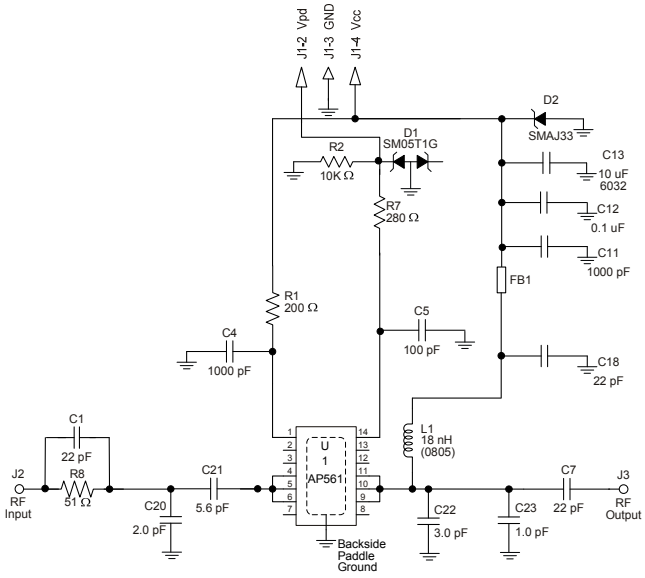
Performance Plots – AP561-PCB2140

Test conditions unless otherwise noted: V_{CC} = +12 V, V_{PD} = +5 V, I_{CQ} = 350 mA (typ.), Temp=+25°C



AP561-PCB2350 Evaluation Board (2300−2400 MHz)





Notes:

1. See Evaluation Board PCB Information section for material and stack-up.
2. All components are of 0603 size unless stated on the schematic.
3. The right edge of C20 is placed at 123 mil from the AP561 RFin pin.
4. The right edge of C21 is placed at 45 mil from the AP561 RFin pin.
5. The left edge of C22 is placed at 30 mil from the AP561 RFout pin.
6. The left edge of C23 is placed at 280 mil from the AP561 RFout pin.
7. Do not exceed 5.5V on Vpd or damage to D1 will occur. Do not exceed 13V on Vcc or damage to D2 will occur.
8. The primary RF microstrip line is 50 Ω. The RF trace is cut at component C21 for this particular reference design.

Bill of Material – AP561-PCB2350

Reference Des.	Value	Description	Manuf.	Part Number
N/A	N/A	Printed Circuit Board – FR4		
U1	N/A	0.7-2.9 GHz 8W Power Amplifier	TriQuint	AP561-F
C1, C7, C18	22 pF	Cap, Chip, 0603, 50V, 5%, NPO	various	
C5	100 pF	Cap, Chip, 0603, 50V, 5%, NPO	various	
C4, C11	1000 pF	Cap, Chip, 0603, 50V, 5%, NPO	various	
C12	0.1 uF	Cap, Chip, 0603, 50V, 5%, NPO	various	
C13	10 uF	Cap, Tantalum, 6032, 35V, 10%	various	
R2	10 KΩ	Resistor, Chip, 0603, 5%, 1/16W	various	
R7	280 Ω	Resistor, Chip, 0603, 1%, 1/16W	various	
R1	200 Ω	Resistor, Chip, 0805, 1%, 1/16W	various	
FB1	N/A	Ferrite Bead, 100 MHz	various	
C22	3.0 pF	Cap, Chip, 0603, 50V, +/-0.05pF	AVX	06035J3R0ABSTR
C21	5.6 pF	Cap, Chip, 0603, 50V, +/-0.05pF	AVX	06035J5R6ABSTR
C23	1.0 pF	Cap, Chip, 0603, 50V, +/-0.05pF	AVX	06035J1R0ABSTR
C20	2.0 pF	Cap, Chip, 0603, 50V, +/-0.05pF	AVX	06035J2R0ABSTR
L1	18 nH	Ind, Chip, 0805, 5%, Ceramic	Coilcraft	0805HQ-18NXJC
R8	51 Ω	Resistor, Chip, 0603, 1%, 1/16W	various	
D1	N/A	TVS Diode Array, 5V, SOT23, 2Ch	On-Semiconductor	SM05T1G
D2	N/A	Diode TVS, 33V, 400W, 5% SMA	On-Semiconductor	1SMA33AT3G

Typical Performance – AP561-PCB2350

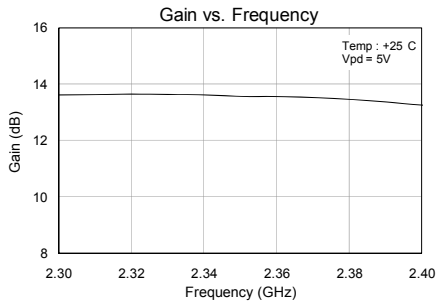
Test conditions unless otherwise noted: V_{CC} = +12 V, V_{PD} = +5 V, I_{CQ} = 340 mA (typ.), Temp=+25°C

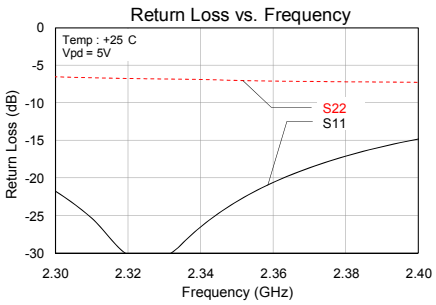
Parameter	Typical Values			Units
Frequency	2300	2350	2400	MHz
Gain	13.6	13.6	13.2	dB
Input Return Loss	21	23	14	dB
Output Return Loss	6.6	7	7	dB
EVM @ 28dBm Output Power [1]	1.6	1.4	1.1	%
ACLR @ 28dBm Output Power [2]	-45.8	-47.0	-48.7	dBc
Operating Current, I_{CC} @ 28dBm Output Power [2]	500	475	465	mA
Collector Efficiency @ 28dBm Output Power [2]	10.7	11.1	11.5	%
Output P1dB	40.1	39.5	39.0	dBm

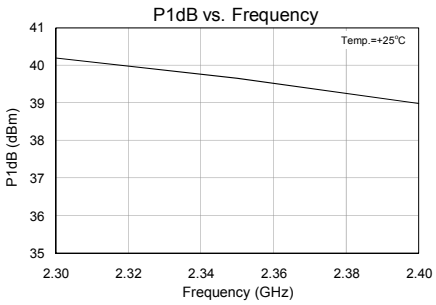
Notes:
1. 802.16-2004 O-FDMA, 64QAM-1/2, 1024-FFT, 20 symbols and 30 subchannels.10.2dB PAR @ 0.01%, 3.84 MHz Carrier BW
2. ACLR test set-up: 3GPP WCDMA, TM1+64DPCH, +5MHz Offset, PAR = 10.2 dB @ 0.01% Probability.

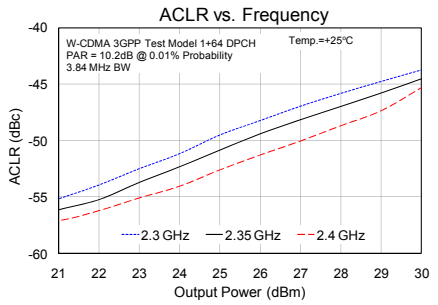
Performance Plots – AP561-PCB2350

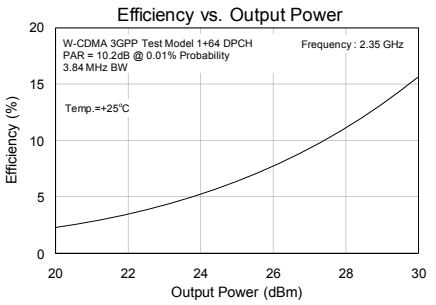
Test conditions unless otherwise noted: V_{CC} = +12 V, V_{PD} = +5 V, I_{CQ} = 340 mA (typ.), Temp=+25°C

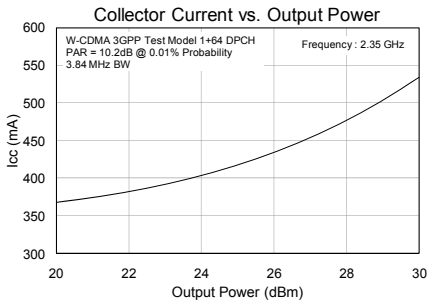


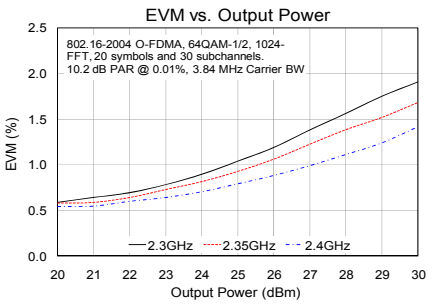




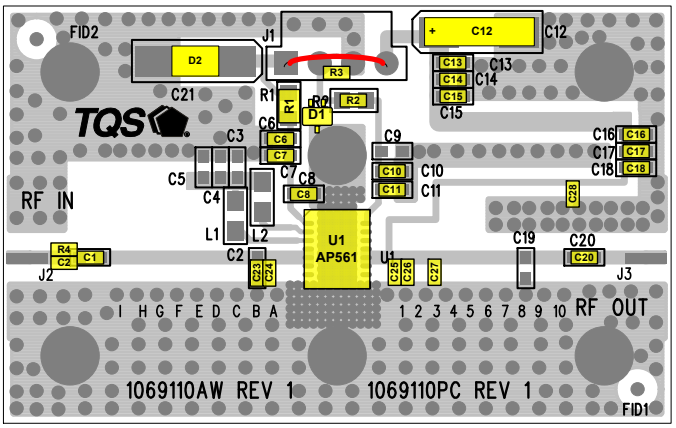


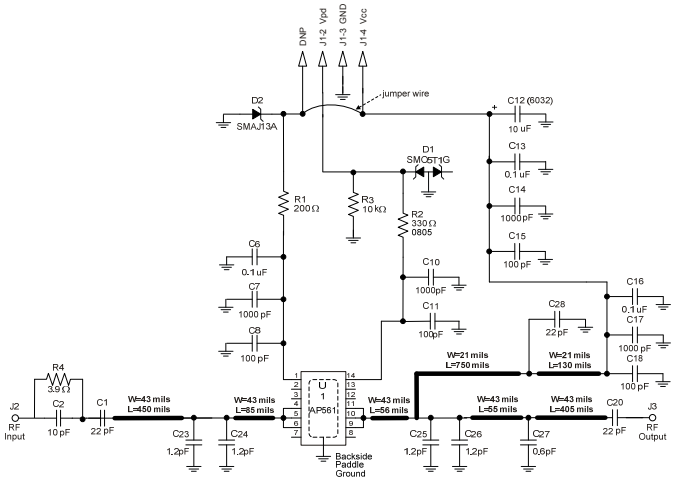






AP561-PCB2500 Evaluation Board (2500−2700 MHz)





Notes:

1. See Evaluation Board PCB Information section for material and stack-up.
2. All components are of 0603 size unless stated on the schematic.
3. The right edge of C24 is placed at 85 mil from the AP561 RFin pin.
4. The left edge of C25 is placed at 55 mil from the AP561 RFout pin.
5. The left edge of C27 is placed at 175 mil from the AP561 RFout pin.
6. The DC bias feed is approximately a ¼ λ from output RF trace to C28.
7. Do not exceed 5.5V on Vpd or damage to D1 will occur. Do not exceed 13V on Vcc or damage to D2 will occur.
8. The primary RF microstrip line is 50Ω. The RF trace is cut at component C21 for this particular reference design.

Bill of Material – AP561-PCB2500

Reference Des.	Value	Description	Manuf.	Part Number
N/A	N/A	Printed Circuit Board – Ultralam		
U1	N/A	0.7-2.9 GHz 8W Power Amplifier	TriQuint	AP561-F
C6, C16	0.1 uF	CAP, 0603,10%, 50V, X7R	various	
C7, C10, C17	1000 pF	CAP, 0603, 5%, 50V, NPO	various	
C8, C11, C18	100 pF	CAP, 0603, 5%, 50V, NPO	various	
C12	10 uF	CAP, 1206, 10%, 15V, Tantalum	various	
R1	200 Ω	RES, 0805, 5%, 1/10W. Chip	various	
R2	330 Ω	RES, 0603,5%, 1/10W, Chip	various	
R3	10 kΩ	RES, 0603, 5%,1/16W, Chip	various	
C1, C20, C28	22 pF	CAP, 0603, 5%, 50V, NPO/COG	various	
C23, C24, C25, C26	1.2 pF	CAP, 0603, ± 0.05 pF, ACCU-P, 50V	AVX	06035J1R2ABSTR
C2	10 pF	CAP, 0603, 5%, 50V, NPO	various	
C27	0.6 pF	CAP, 0603, ± 0.05 pF, ACCU-P, 50V	AVX	06035J0R6ABSTR
R4	3.9 Ω	RES, 0603, 5%, 1/16W, Chip	various	
D1	N/A	TVS Diode Array, 5V, SOT23, 2Ch	On-Semiconductor	SM05T1G
D2	N/A	Diode TVS, 13V	On-Semiconductor	1SMA33AT3G

Typical Performance – AP561-PCB2500

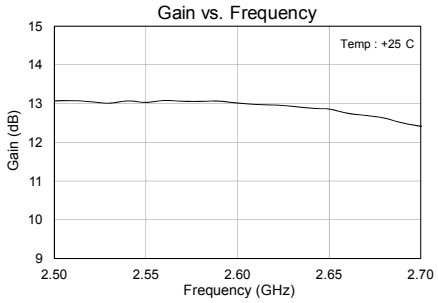
Test conditions unless otherwise noted: V_{CC} = +12 V, V_{PD} = +5 V, I_{CQ} = 300 mA (typ.), Temp=+25°C

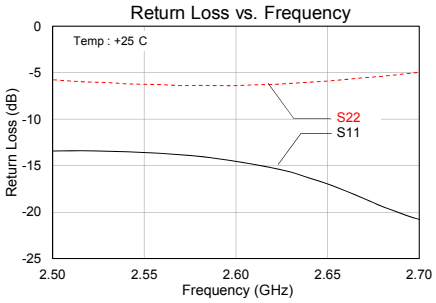
Parameter	Typical Values			Units
Frequency	2500	2600	2700	MHz
Gain	13.1	13.0	12.4	dB
Input Return Loss	13	14.5	20	dB
Output Return Loss	5.8	6.5	5	dB
EVM @ 30dBm Output Power [1]	2.1	1.7	1.4	%
Operating Current, I_{CC} @ 30dBm Output Power [1]	545	510	500	mA
Collector Efficiency @ 30dBm Output Power [1]	15.2	16.2	16.8	%
Output P1dB	39.8	39.0	38.0	dBm

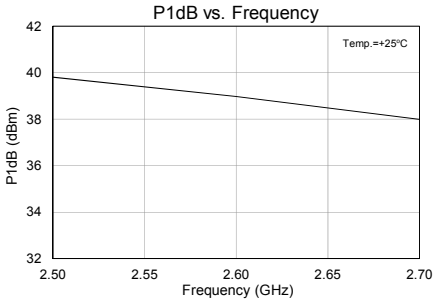
Notes:
1. 802.16-2004 O-FDMA, 64QAM-1/2, 1024-FFT, 20 symbols and 30 subchannels.PAR = 10.2dB@ 0.01%, 3.84 MHz Carrier BW
2. W-CDMA 3GPP, TM1+64DPCH, +5MHz Offset, PAR = 10.2 dB @ 0.01%, 3.84MHz BW

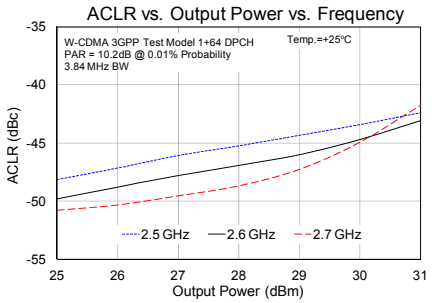
Performance Plots – AP561-PCB2500

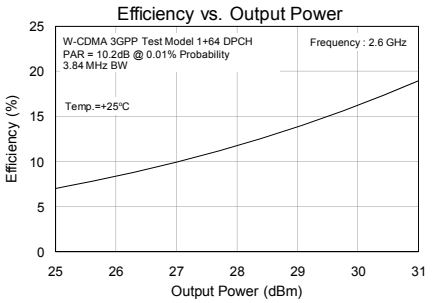
Test conditions unless otherwise noted: V_{CC} = +12 V, V_{PD} = +5 V, I_{CQ} = 300 mA (typ.), Temp=+25°C

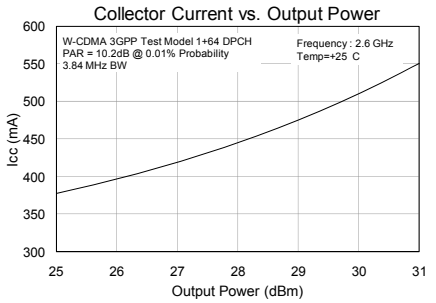


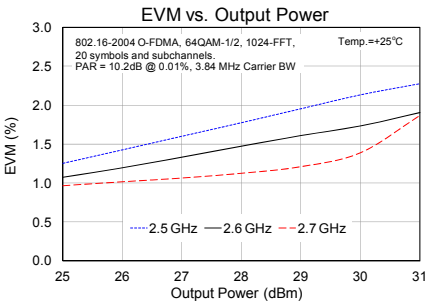










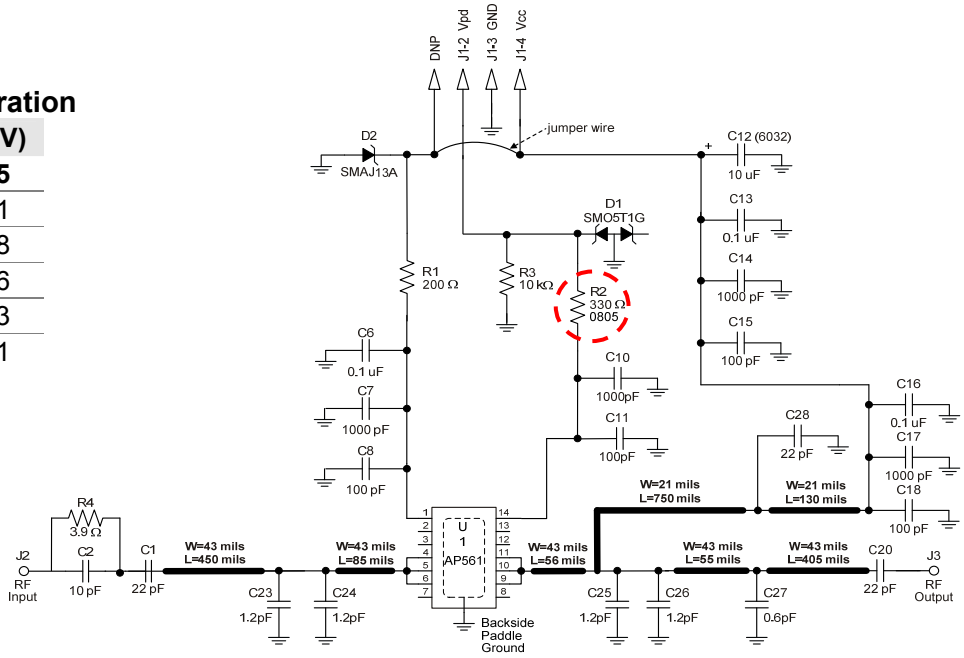


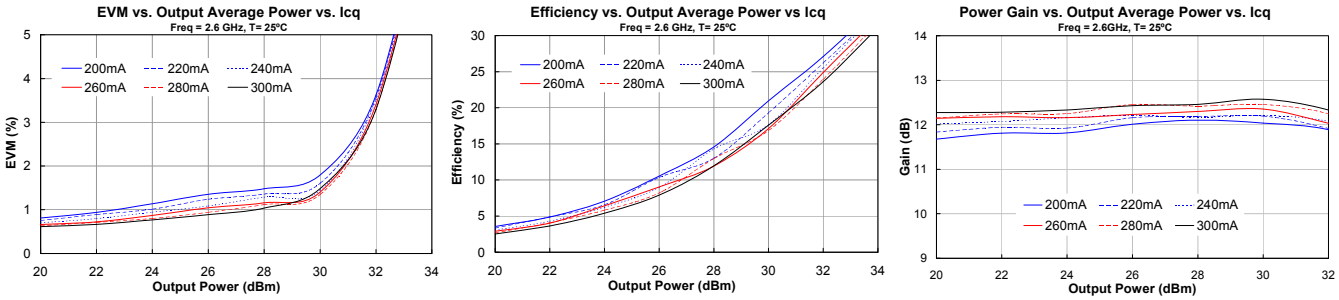
Reference Design 2500-2700 MHz: Changing Icq Biasing Configurations

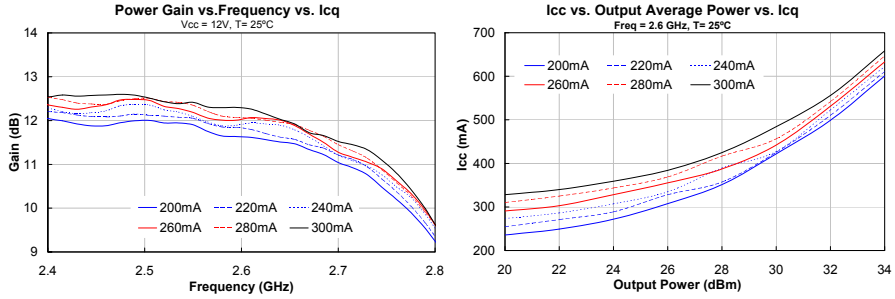
The AP561 can be configured to operate with lower bias current by varying the bias-adjust resistor R2. (**Error! Not a valid bookmark self-reference.**) The recommended circuit configuration has the device operating with a 300 mA as the quiescent current (I_{CQ}). This biasing level represents a tradeoff in terms of EVM and efficiency. Lowering I_{CQ} will improve upon the efficiency of the device, but degrade the EVM performance. Measured data shown in the plots below represents the AP561-PCB2500 measured and configured for 2.6GHz applications. It is expected that variation of the bias current for other frequency applications will produce similar performance results.

Table 1 : Reduced Current Operation

I_{CQ} (mA)	R2 (Ω)	V_{PD} (V)	I_{REF} (V)
300	**330**	**5**	**2.85**
280	336	5	2.81
260	340	5	2.78
240	343	5	2.76
220	348	5	2.73
200	351	5	2.71



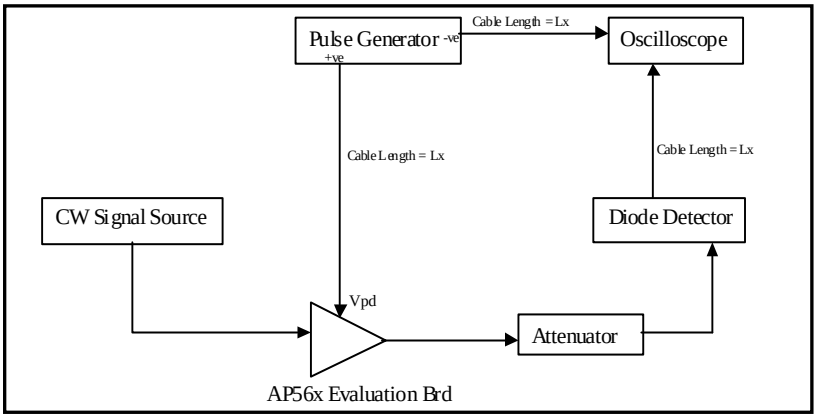




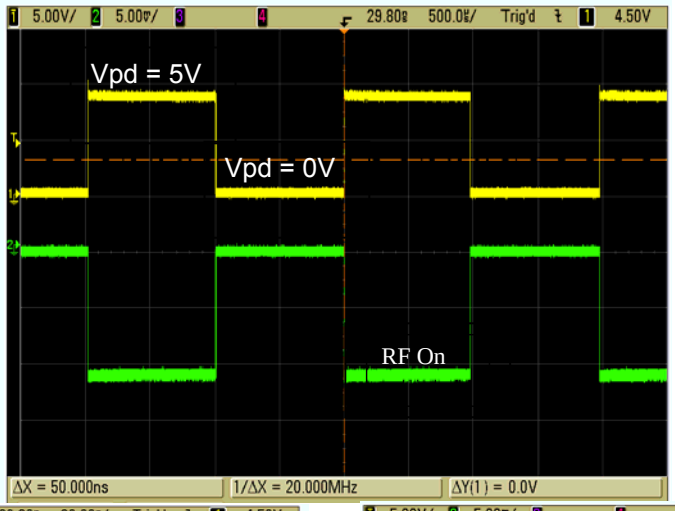
Parameter Measurement Information: Switching Speed Test

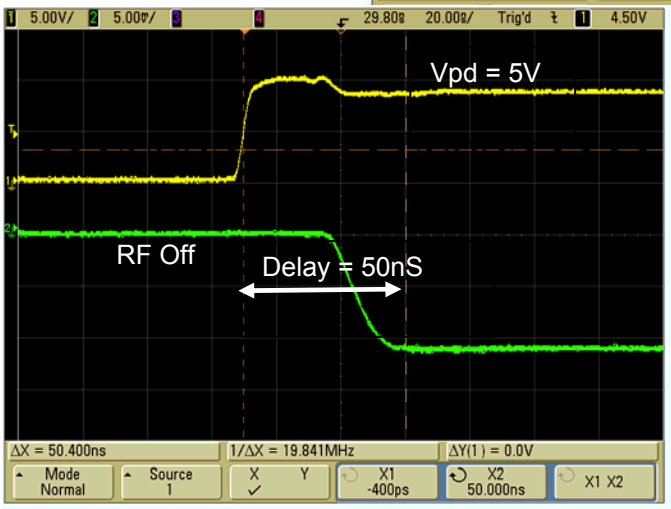
Test Conditions:

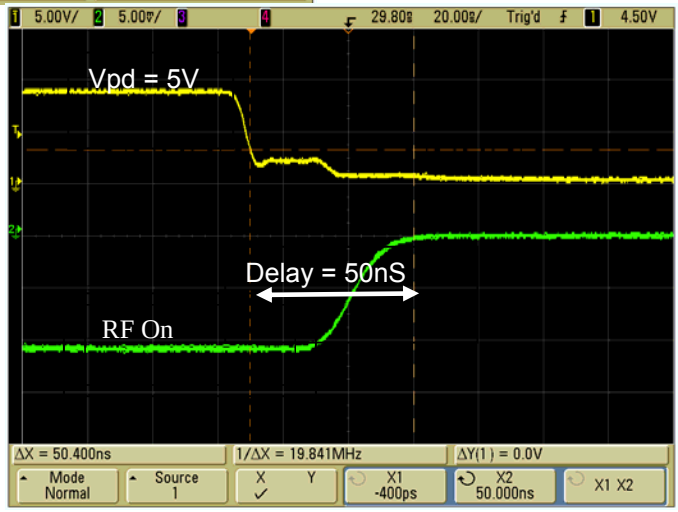
V_{cc} = +12V at 25°C
Output Power = +30dBm at 2.5 GHz
Rep Rate = 1 KHz, 50% duty cycle
Vpd amplitude = +5V
R2 = 200Ω, C9 = 12pF
(C10, C11 removed for best switching performance)
Xtal Detector Voltage =15mV (square law)



Test Result Waveforms:







Evaluation Board Bias Procedure

Following bias procedure is recommended to ensure proper functionality of AP561 in a laboratory environment. The sequencing is not required in the final system application.

Bias.	Voltage (V)
V_{CC}	+12
V_{PD}	+5

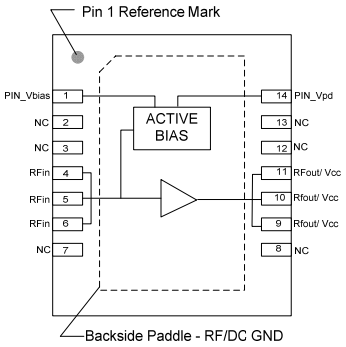
Turn-on Sequence:

1. Attach input and output loads onto the evaluation board.
2. Turn on power supply V_{CC} = +12V.
3. Turn on power supply V_{PD} = +5V.
4. Turn on RF power.

Turn-off Sequence:

1. Turn off RF power.
2. Turn off power supply V_{PD} = +5V.
3. Turn off power supply V_{CC} = +12V.

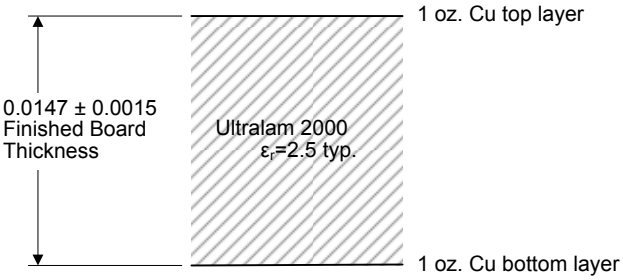
Pin Configuration and Description

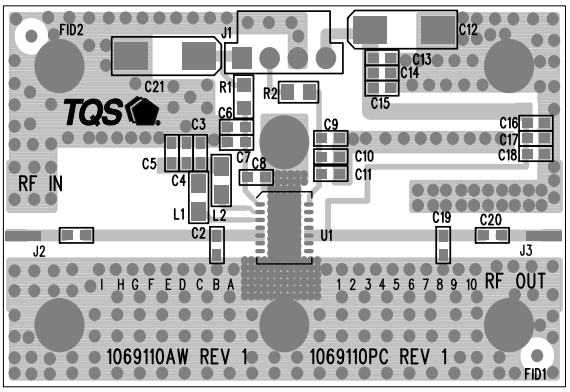


Pin No.	Label	Description
1	PIN_V_{BIAS}	Voltage supply for active bias for the amp. Connect to same supply voltage as Vcc.
2, 3, 7, 8, 12, 13	N/C	No internal connection. This pin can be grounded or N/C on PCB. Land pads should be provided for PCB mounting integrity.
4, 5, 6	RF IN	RF Input. DC Voltage present, blocking cap required. Requires matching for operation.
9, 10, 11	RF Output / V_{CC}	RF Output. DC Voltage present, blocking cap required
14	PIN_V_{PD}	Reference current into internal active bias current mirror. Current into PIN_VPD sets device quiescent current. Also, can be used as on/off control.
Backside Paddle	RF/DC GND	Multiple Vias should be employed to minimize inductance and thermal resistance. Use recommended via pattern shown under mounting configuration and ensure good solder attach for optimum thermal and electrical performance

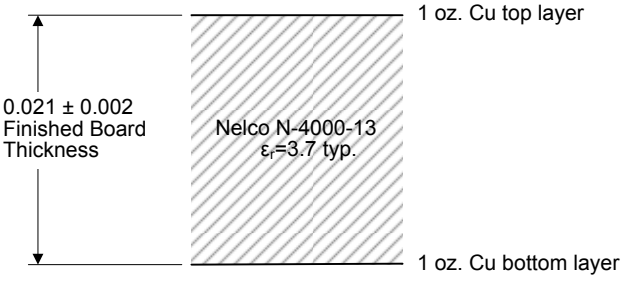
Evaluation Board PCB Information

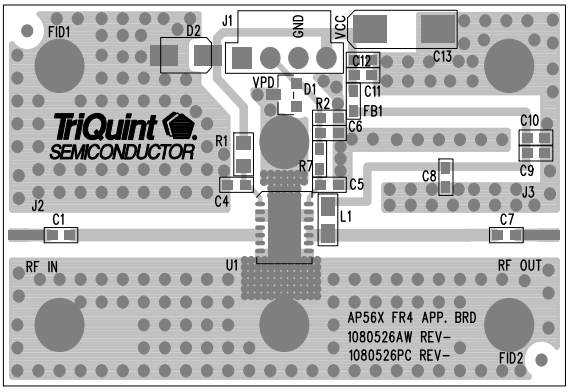
TriQuint PCB 1069110 Material and Stack-up
Ultralam





TriQuint PCB 1080526 Material and Stack-up
FR4

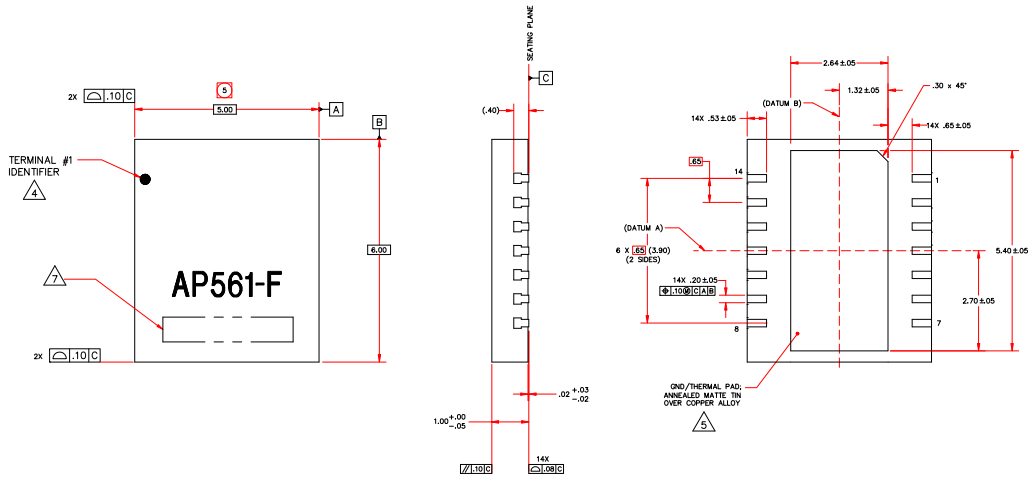




Mechanical Information

Package Marking and Dimensions

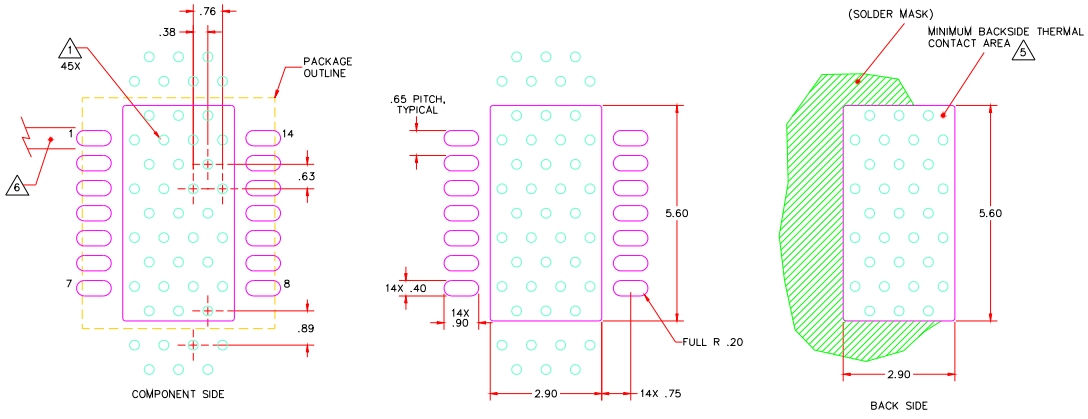
Marking: Part number – AP561-F
Lot code – XXXX



Notes:

1. All dimensions are in millimeters. Angles are in degrees.
2. Except where noted, this part outline conforms to JEDEC standard MO-220, Issue E (Variation VGGC) for thermally enhanced plastic very thin fine pitch quad flat no lead package (QFN).
3. Dimension and tolerance formats conform to ASME Y14.4M-1994.
4. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.

PCB Mounting Pattern



Notes:

1. All dimensions are in millimeters. Angles are in degrees.
2. Use 1 oz. copper minimum for top and bottom layer metal.
3. Vias are required under the backside paddle of this device for proper RF/DC grounding and thermal dissipation. We recommend a 0.35mm (#80/.0135") diameter bit for drilling via holes and a final plated thru diameter of 0.25 mm (0.10”).
4. Ensure good package backside paddle solder attach for reliable operation and best electrical performance.

Product Compliance Information

ESD Sensitivity Ratings

Caution! ESD-Sensitive Device

ESD Rating:	Class 1A
Value:	Passes ≥ 250 V to < 500 V
Test:	Human Body Model (HBM)
Standard:	JEDEC Standard JESD22-A114

ESD Rating:	Class IV
Value:	Passes ≥ 1000 V to <2000 V
Test:	Charged Device Model (CDM)
Standard:	JEDEC Standard JESD22-C101

MSL Rating

MSL Rating:	Level 3
Test:	260°C convection reflow
Standard:	JEDEC Standard IPC/JEDEC J-STD-020

Solderability

Compatible with both lead-free (260 °C max. reflow temperature) and tin/lead (245 °C max. reflow temperature) soldering processes.

Contact plating: Annealed Matte Tin over Cu

RoHs Compliance

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

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Email: info-sales@triquint.com **Fax:** +1.503.615.8902

For technical questions and application information: **Email:** sjcapplications.engineering@triquint.com

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