MAAP-000069-PKG003

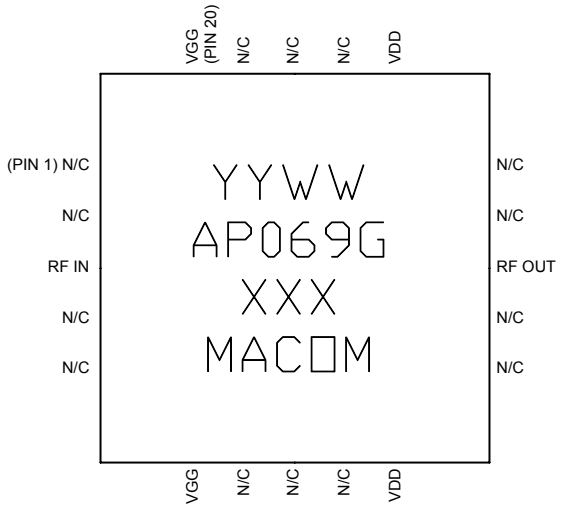
Tyco Electronics

Amplifier, Power, 1.6W
7.7—11.7 GHz

M/A-COM Products
Rev C

Features

- **1.6 Watt Saturated Output Power Level**
- **Variable Drain Voltage (6-10V) Operation**
- **MSAG™ Process**
- **RoHS Compliant**



Description

The MAAP-000069-PKG003 is a 4-stage 1.6W power amplifier with on-chip bias networks in a 20 lead MLP package, allowing easy assembly. This product is fully matched to 50 ohms on both the input and output. It can be used as a power amplifier stage or as a driver stage in high power applications.

Each device is 100% RF tested to ensure performance compliance. The part is fabricated using M/A-COM's GaAs Multifunction Self-Aligned Gate (MSAG) Process.

The 5 mm PQFN package has a lead-free lead finish that is RoHS compliant and compatible with a 260°C reflow temperature. The package also features low lead inductance and an excellent thermal path. The MTTF is 1,000,000 hours at 170°C.

Primary Applications

- **Point-to-Point Radio**
  - **7, 8 and 11 GHz Bands**

Ordering Information

Description	Die	Tape & Reel (500)	Tape & Reel (1000)	Packaged Sample Board
Part Number	MAAPGM0069-DIE	MAAP-000069-TR0500	MAAP-000069-TR1000	MAAP-000069-SMB003

Electrical Characteristics: T_B = 30°C[1], Z_0 = 50 Ω, V_{DD} = 8V, I_{DQ} = 750mA[2], P_{in} = 6 dBm, R_G = 100 Ω

Parameter	Symbol	Min	Typical	Max	Units
Bandwidth	f	7.7		11.7	GHz
Output Power	P_{OUT}	30	32		dBm
1-dB Compression Point	P1dB		31.5		dBm
Power Added Efficiency	PAE		20		%
Small Signal Gain	G	24	27		dB
Input VSWR	VSWR		1.3:1		
Output VSWR	VSWR		2.7:1		
Gate Current	I_{GG}		6		mA
Drain Current	I_{DD}		1.1	1.3	A
Output Third Order Intercept P_{out} = 18 dBm (SCL)	TOI	40	40.5		dBm
Output Third Order Intermod, P_{out} = 18 dBm (SCL)	IM3		45		dBc

1. **T_B = MMIC Case Temperature**
2. **Adjust V_{GG} between –2.7 and –1.2V to achieve specified Idq.**

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Maximum Ratings[3]

Parameter	Symbol	Absolute Maximum	Units
Input Power	P_{IN}	11.0	dBm
Drain Supply Voltage	V_{DD}	+12.0	V
Gate Supply Voltage	V_{GG}	-3.0	V
Quiescent Drain Current (No RF)	I_{DQ}	1.2	A
Quiescent DC Power Dissipated (No RF)	P_{DISS}	12	W
Junction Temperature	T_J	170	°C
Storage Temperature	T_{STG}	-55 to +150	°C

3. Operation beyond these limits may result in permanent damage to the part.

Recommended Operating Conditions[4]

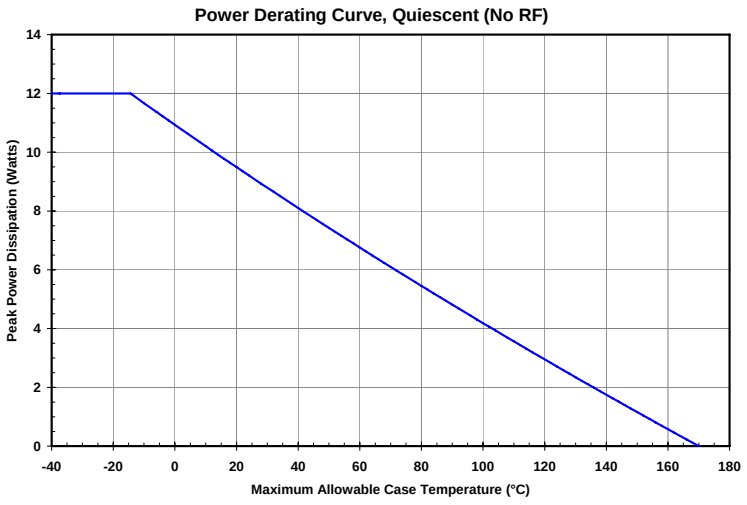
Characteristic	Symbol	Min	Typ	Max	Unit
Drain Voltage	V_{DD}	6.0	8.0	10.0	V
Gate Voltage	V_{GG}	-2.7	-2.0	-1.2	V
Input Power	P_{IN}		6.0	8.0	dBm
Thermal Resistance	Θ_{JC}		16.7		°C/W
MMIC Case Temperature	T_B			Note 5	°C

4. Operation outside of these ranges may reduce product reliability.
5. MMIC Case Temperature = 170°C — Θ_{JC}* V_{DD} * I_{DQ}

Operating Instructions

This device is static sensitive. Please handle with care. To operate the device, follow these steps.

1. Apply V_{GG} = -2.7 V, V_{DD}= 0 V.
2. Ramp V_{DD} to desired voltage, typically 8.0 V.
3. Adjust V_{GG} to set I_{DQ}, (approximately @ –2.0 V).
4. Set RF input.
5. Power down sequence in reverse. Turn V_{GG} off last.



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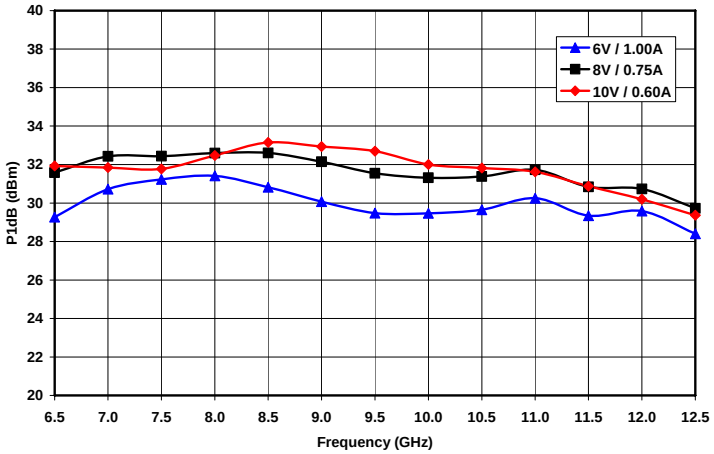

Figure 1. P1dB vs. Frequency and Quiescent Bias Condition (VDD / IDQ)

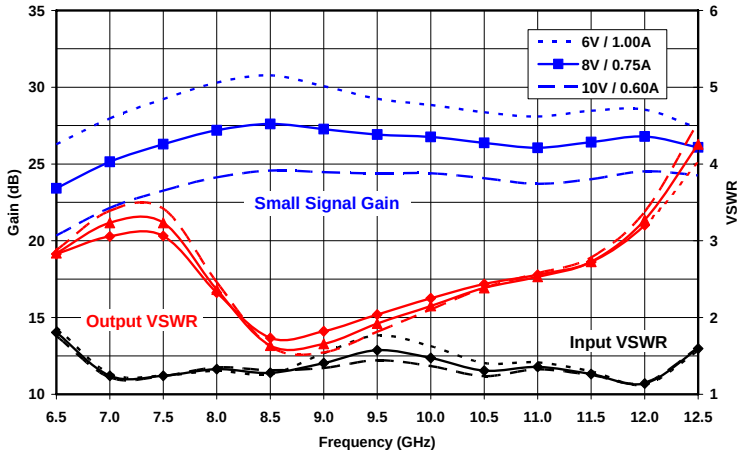

Figure 2. Small Signal Gain and Input & Output VSWR vs. Frequency and Quiescent Bias (Vdd / IDQ)

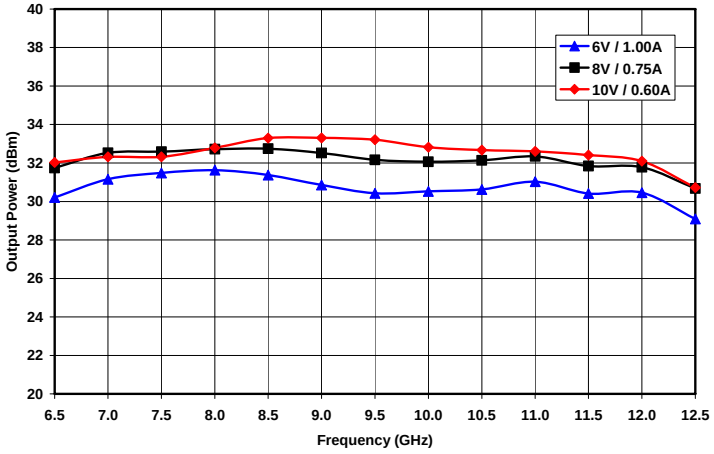

Figure 3. Saturated Output Power vs. Frequency and Quiescent Bias Condition (VDD / IDQ)

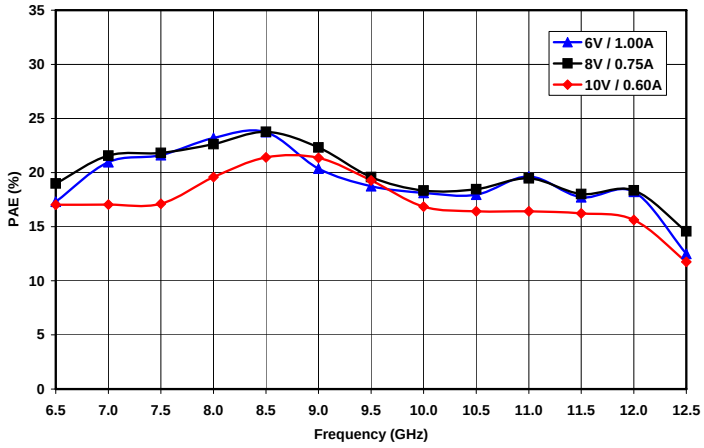

Figure 4. Saturated Power Added Efficiency vs. Frequency and Quiescent Bias Condition (VDD / IDQ)

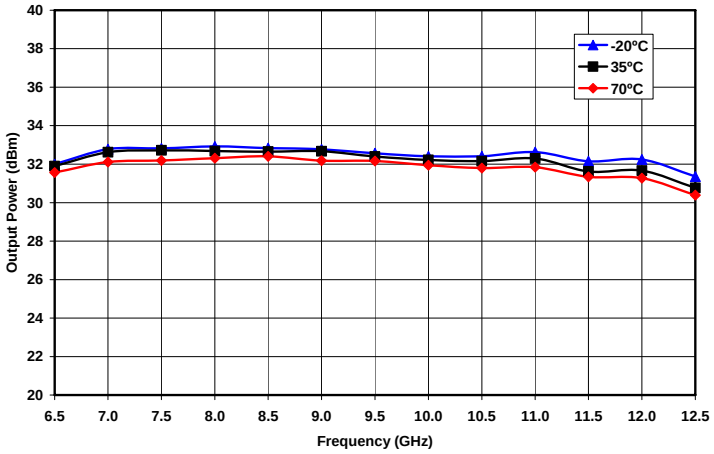

Figure 5. Saturated Output Power vs. Frequency and Case Temperature at VD = 8V and IDQ = 0.75A

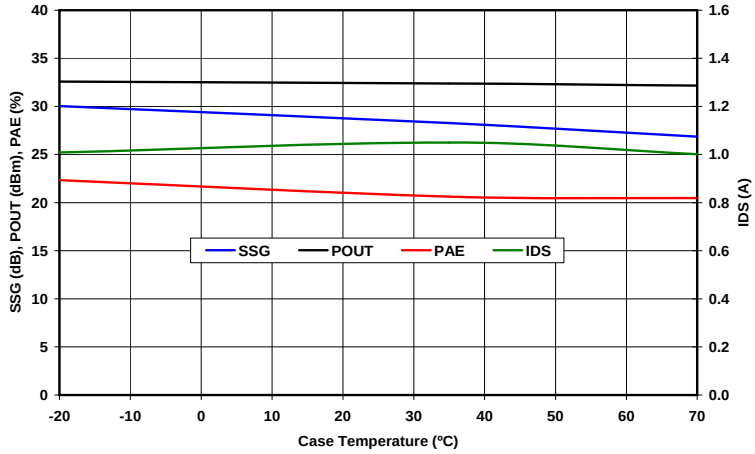

Figure 6. Small Signal Gain & Saturated Output Power, Power Added Efficiency and Drain Current vs. Case Temperature at 9.5 GHZ, VD = 8V, and IDQ = 0.75A

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VD = 6V

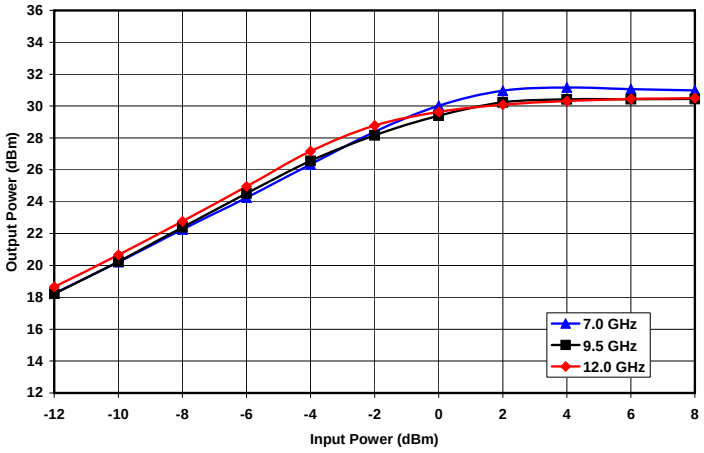

Figure 7. Output Power vs. Input Power and Frequency
at VD = 6V and IDQ = 1.00A

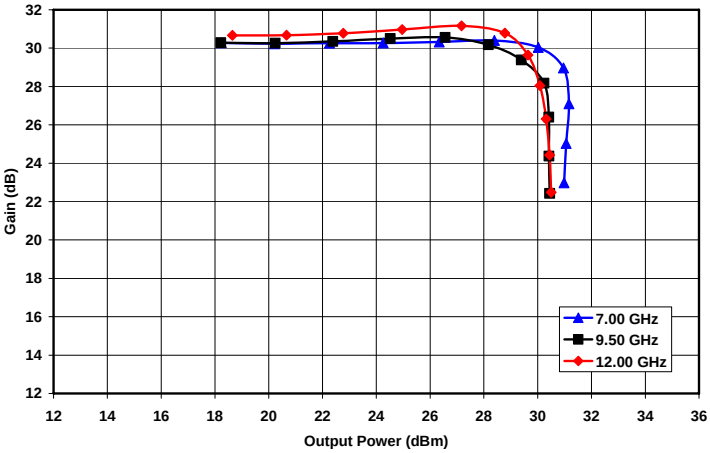

Figure 8. Gain vs. Output Power and Frequency
at VD = 6V and IDQ = 1.00A

VD = 8V

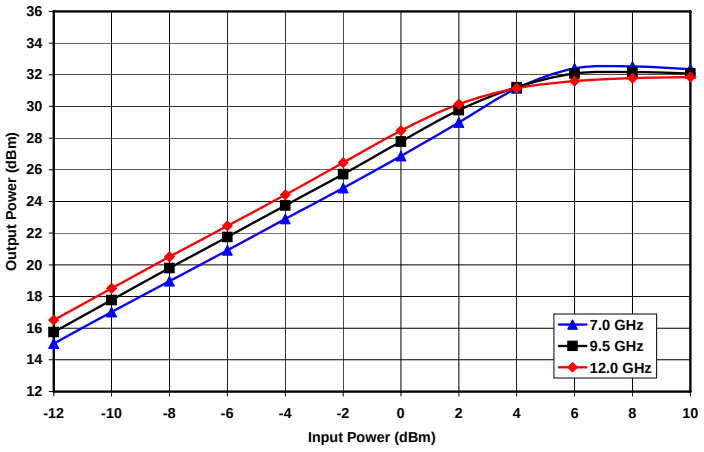

Figure 9. Output Power vs. Input Power and Frequency
at VD = 8V and IDQ = 0.75A

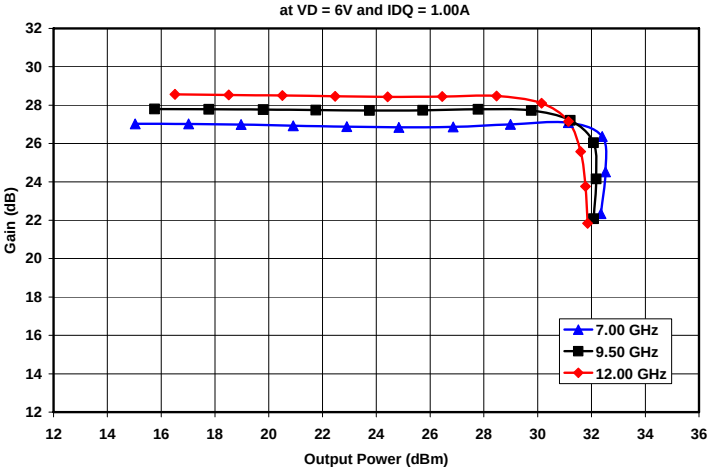

Figure 10. Gain vs. Output Power and Frequency
at VD = 8V and IDQ = 0.75A

VD = 10V

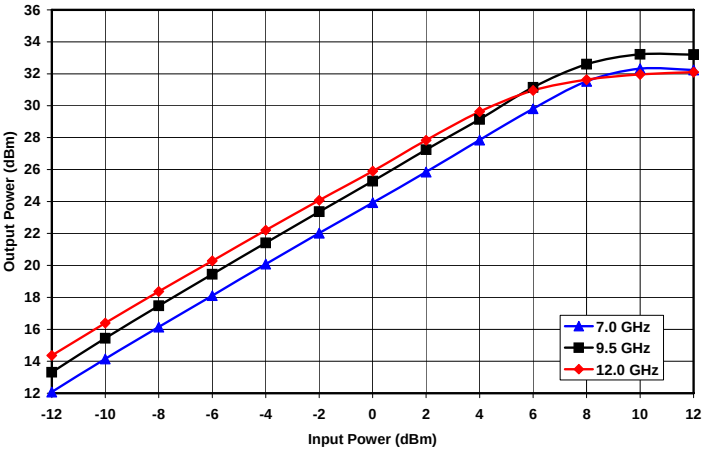

Figure 11. Output Power vs. Input Power and Frequency
at VD = 10V and IDQ = 0.60A

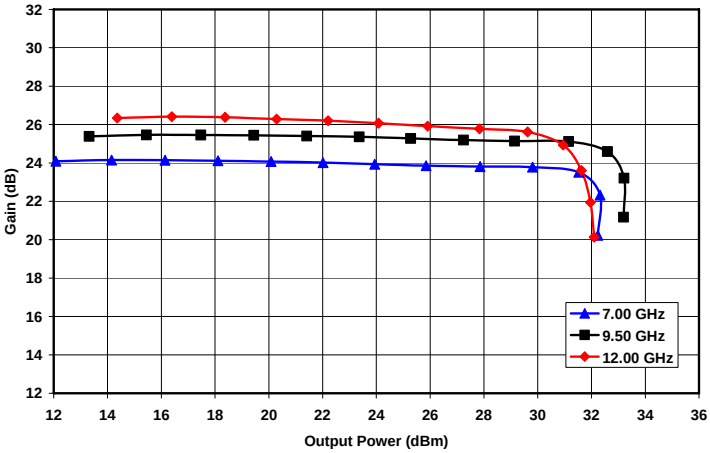

Figure 12. Gain vs. Output Power and Frequency
at VD = 10V and IDQ = 0.60A

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VD = 6V

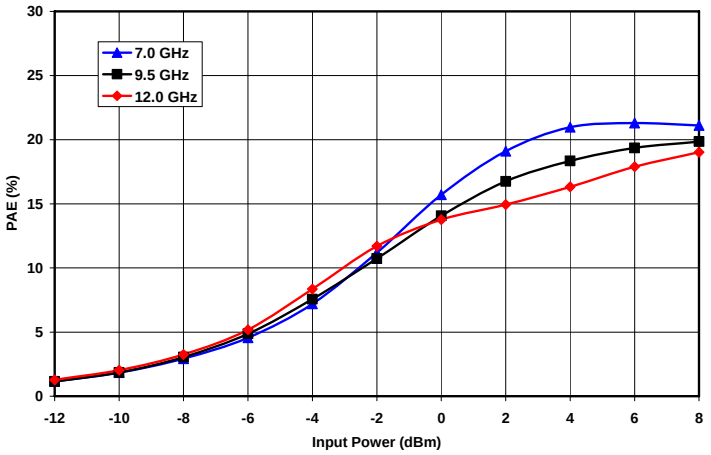

Figure 13. Power Added Efficiency vs. Input Power and Frequency at VD = 6V and IDQ = 1.00A

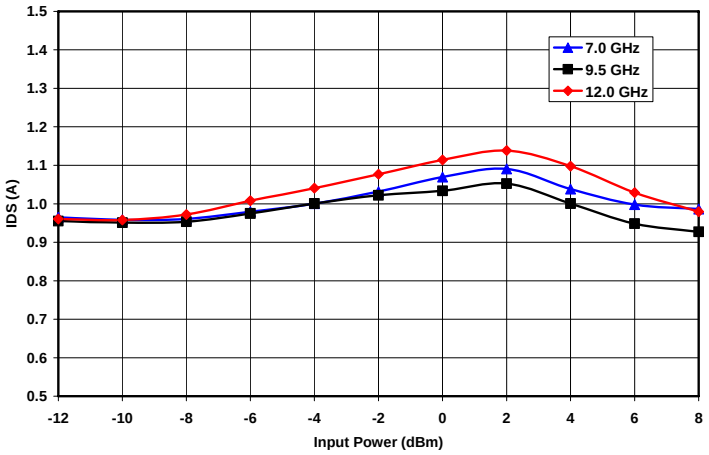

Figure 14. Drain Current vs. Input Power and Frequency at VD = 6V and IDQ = 1.00A

VD = 8V

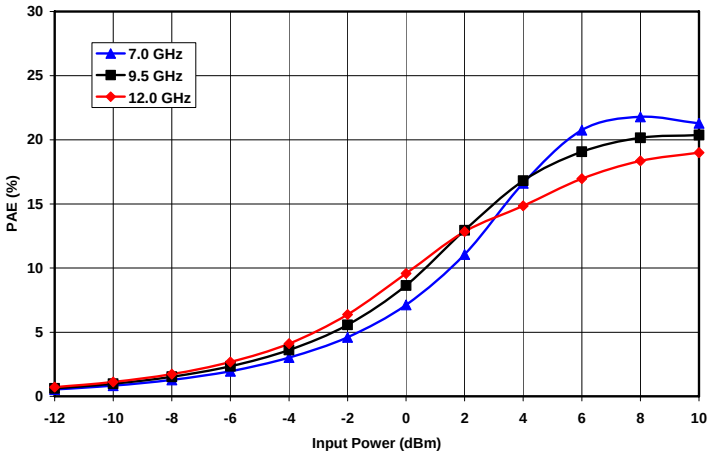

Figure 15. Power Added Efficiency vs. Input Power and Frequency at VD = 8V and IDQ = 0.75A

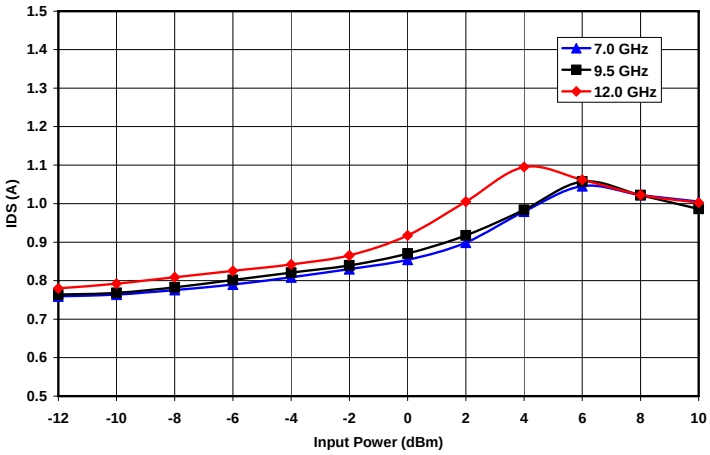

Figure 16. Drain Current vs. Input Power and Frequency at VD = 8V and IDQ = 0.75A

VD = 10V

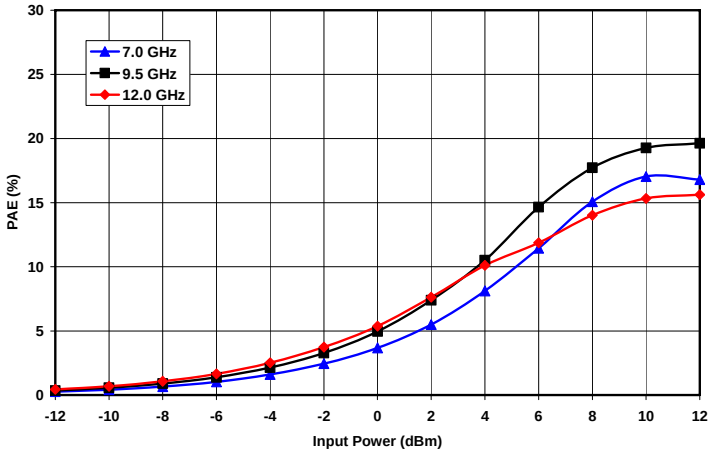

Figure 17. Power Added Efficiency vs. Input Power and Frequency at VD = 10V and IDQ = 0.60A

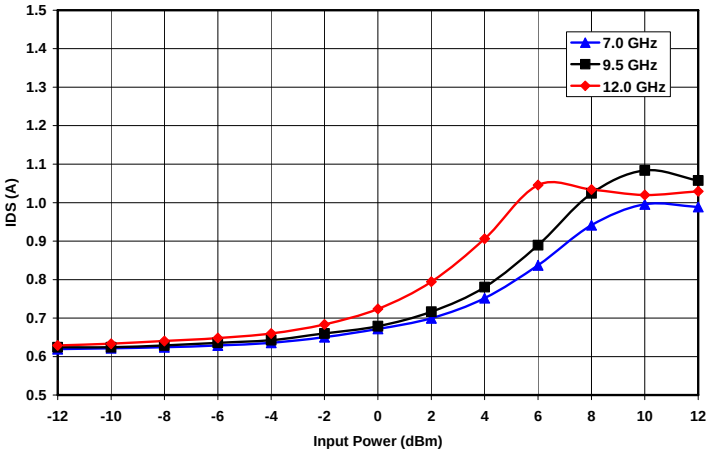

Figure 18. Drain Current vs. Input Power and Frequency at VD = 10V and IDQ = 0.60A

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VD = 6V

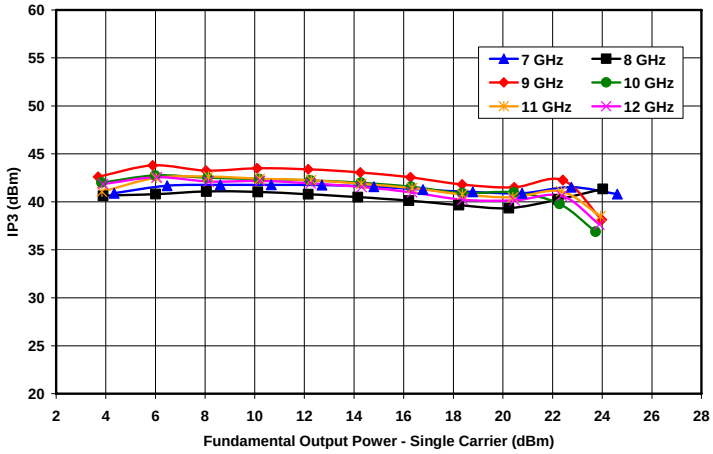

Figure 19. Third Order Intercept vs. Output Power and Frequency at VD = 6V and IDQ = 1.00A

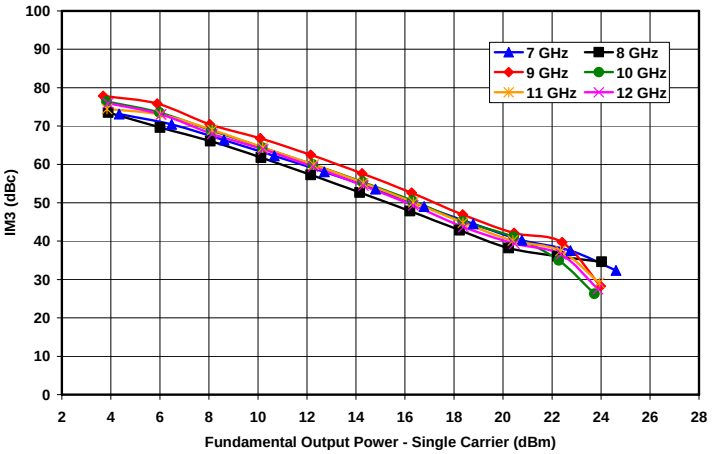

Figure 20. Third Order Intermod vs. Output Power and Frequency at VD = 6V and IDQ = 1.00A

VD = 8V

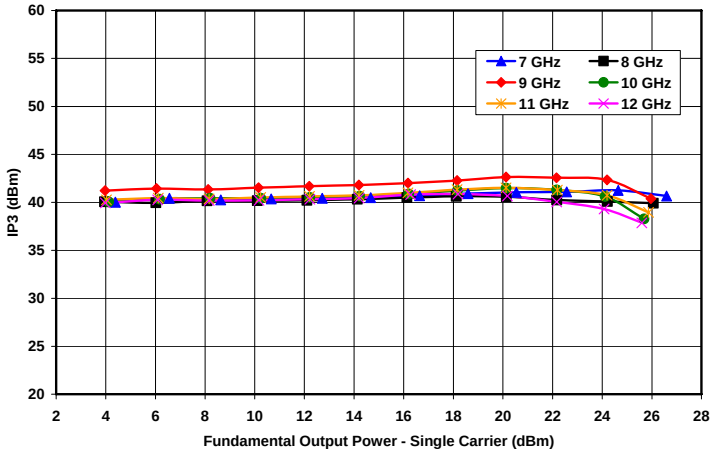

Figure 21. Third Order Intercept vs. Output Power and Frequency at VD = 8V and IDQ = 0.75A

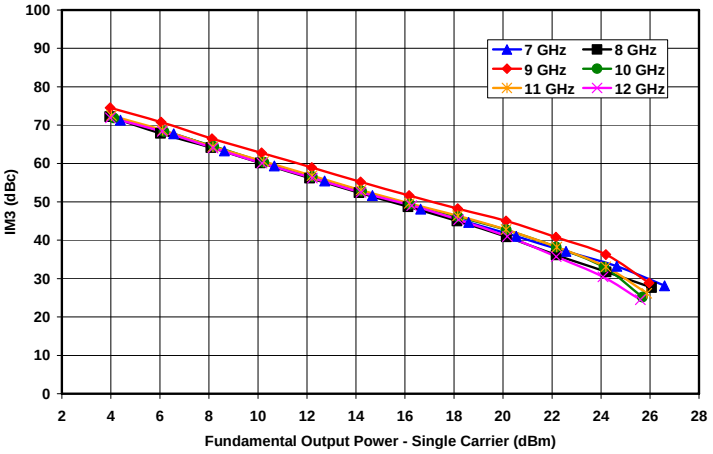

Figure 22. Third Order Intermod vs. Output Power and Frequency at VD = 8V and IDQ = 0.75A

VD = 10V

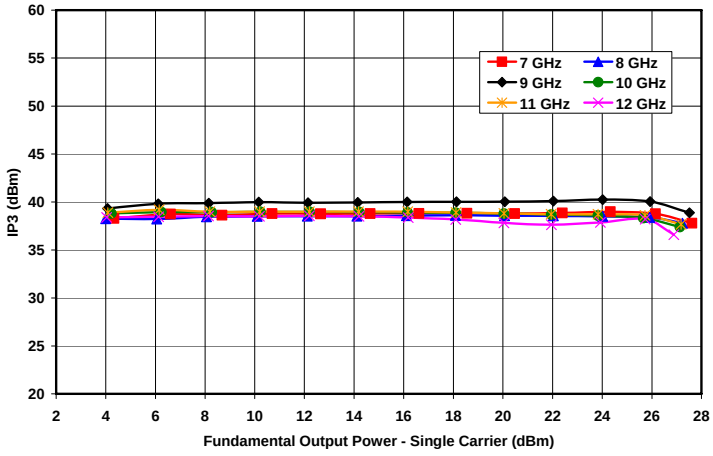

Figure 23. Third Order Intercept vs. Output Power and Frequency at VD = 10V and IDQ = 0.60A

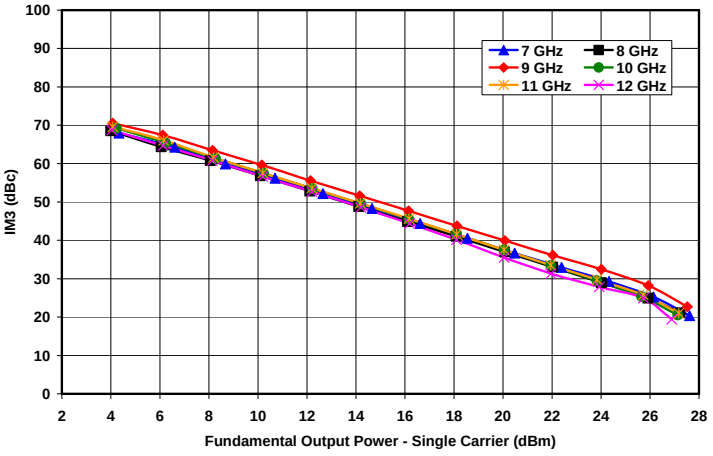

Figure 24. Third Order Intermod vs. Output Power and Frequency at VD = 10V and IDQ = 0.60A

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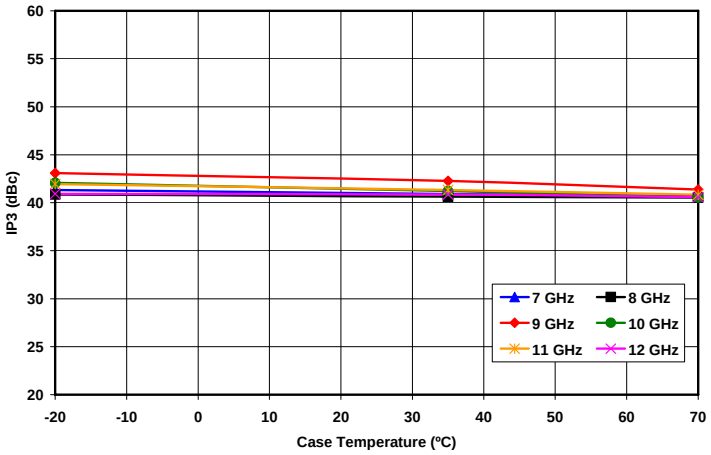

Figure 25. Third Order Intercept vs. Case Temperature and Frequency at Single Carrier Output Power Level = 19dBm, VD = 8V and IDQ = 0.75A

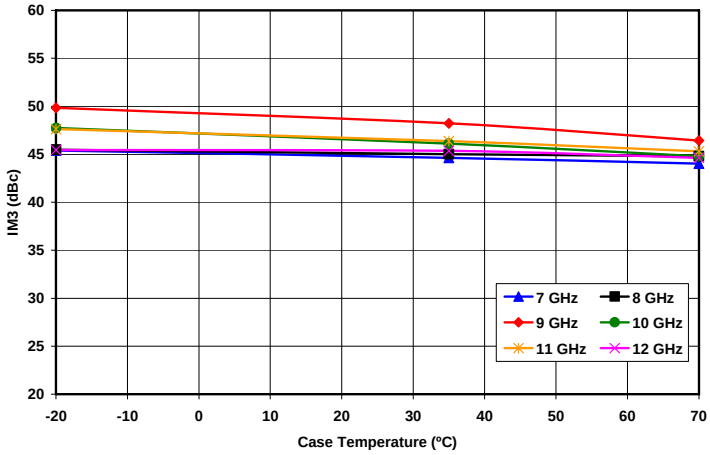

Figure 25. Third Order Intercept vs. Case Temperature and Frequency at Single Carrier Output Power Level = 19dBm, VD = 8V and IDQ = 0.75A

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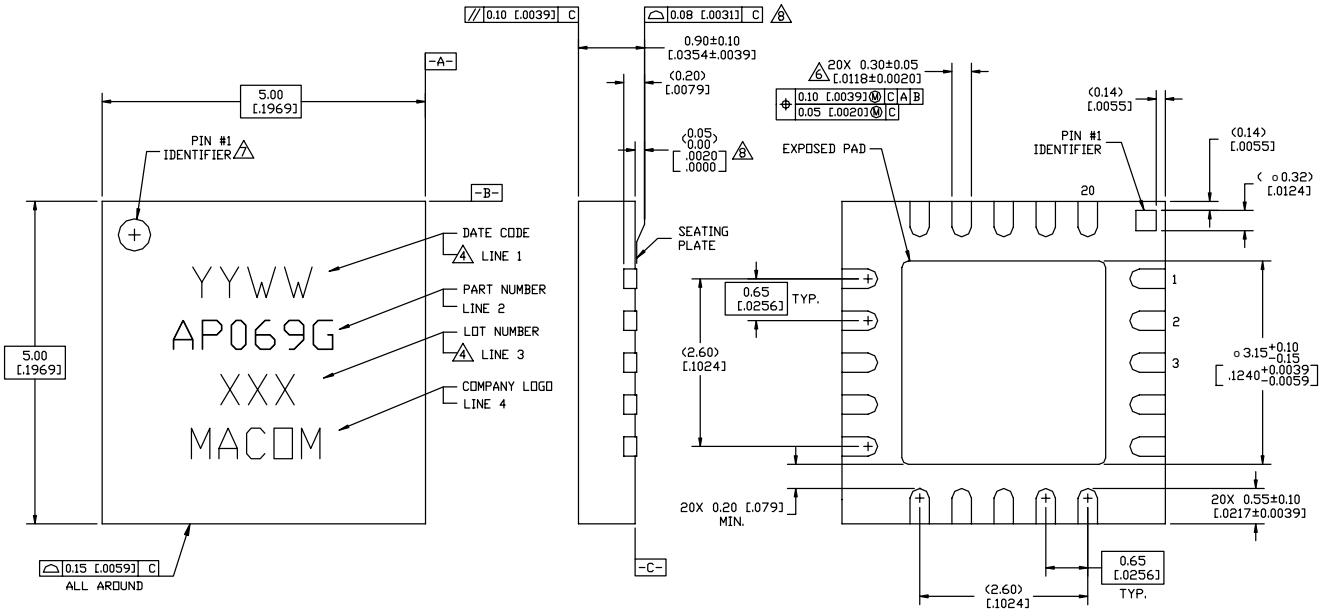

Figure 27. 5x5 mm 20-Lead MLP.

RF ports are internally DC blocked.

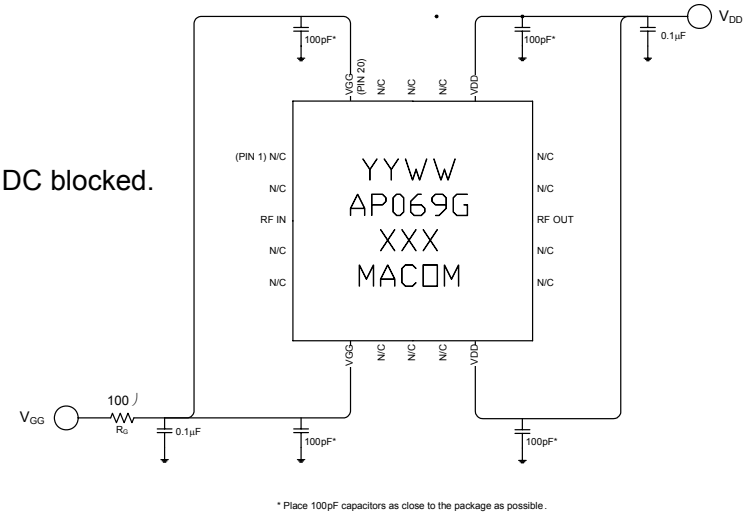

Figure 28. Recommended Bias Configuration.

Note: The exposed pad centered on the package bottom must be connected to RF and dc ground for proper electrical and thermal operation.

Refer to M/A-COM Application Note ***Surface Mounting Instructions for PQFN Packages #S2083**** for assembly guidelines.

Additional Precaution: All parts must receive a bake-out of 125ºC for 24 hours prior to any solder reflow operation.

*Application Notes can be found by going to the Site Search Page of M/A-COM's web page (http://www.macom.com/Application%20Notes/index.htm)) and searching for the required Application Note.

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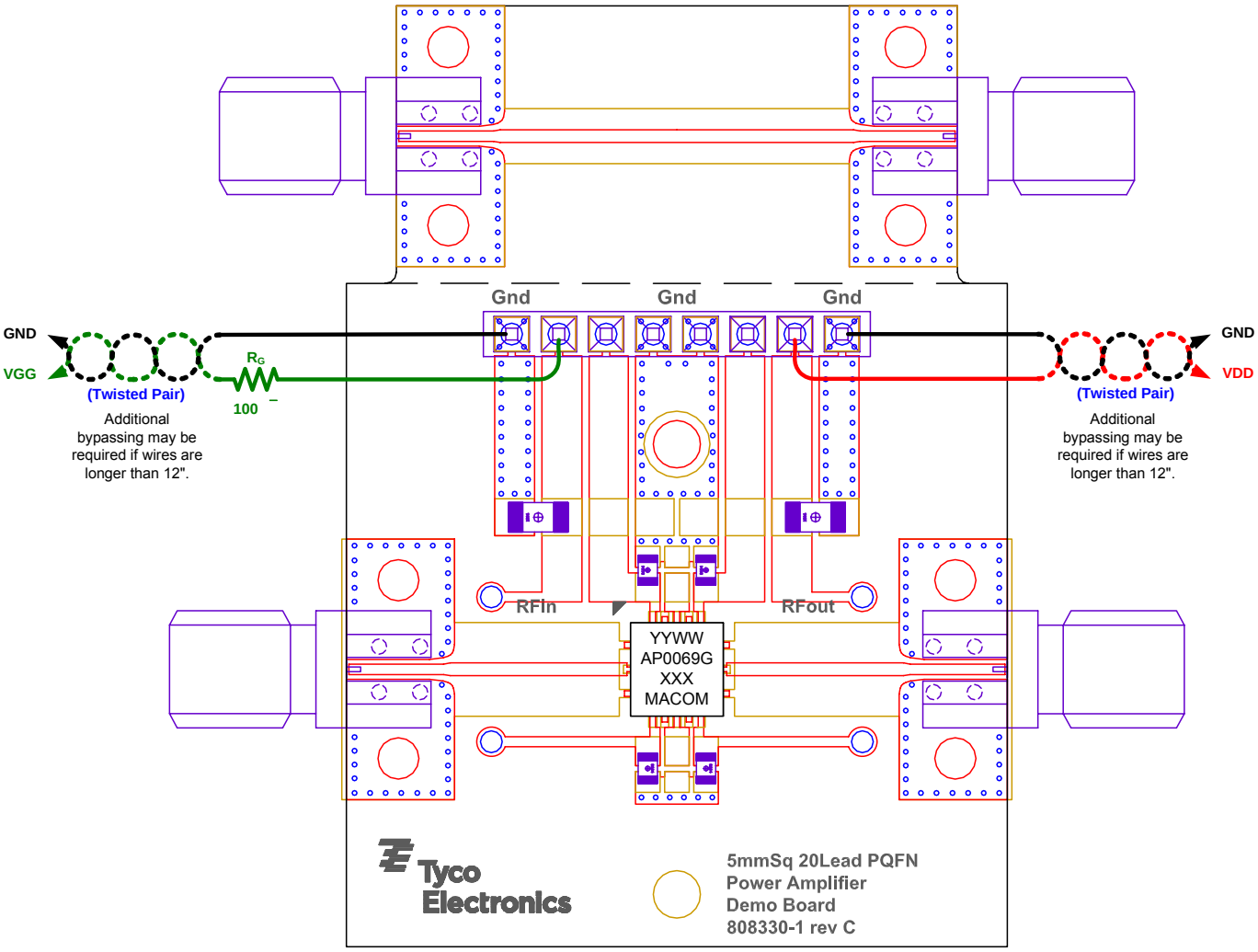

Figure 29. Demonstration Board PN MAAP-000069-SMB003 (available upon request).