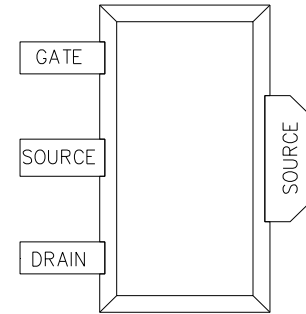


### FEATURES

- ◆ 26 dBm Output Power at 1-dB Compression at 1.8 GHz
- ◆ 17 dB Power Gain at 1.8 GHz
- ◆ 0.7 dB Noise Figure
- ◆ 40 dBm Output IP3 at 1.8 GHz
- ◆ 55% Power-Added Efficiency



### DESCRIPTION AND APPLICATIONS

The LP750SOT89 is a packaged Aluminum Gallium Arsenide / Indium Gallium Arsenide (AlGaAs/InGaAs) pseudomorphic High Electron Mobility Transistor (pHEMT). It utilizes a 0.25  $\mu\text{m}$  x 750  $\mu\text{m}$  Schottky barrier gate, defined by electron-beam photolithography. The recessed “mushroom” gate structure minimizes parasitic gate-source and gate resistance. The epitaxial structure and processing have been optimized for reliable high-power applications. The LP750 also features Si<sub>3</sub>N<sub>4</sub> passivation and is available in die form or in other packages.

Typical applications include drivers or output stages in PCS/Cellular amplifiers, WLL and WLAN systems, and other types of wireless infrastructure systems.

### ELECTRICAL SPECIFICATIONS @ T<sub>Ambient</sub> = 25°C

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Saturated Drain-Source Current LP750SOT89-1	I <sub>DSS</sub>	V <sub>DS</sub> = 2 V; V <sub>GS</sub> = 0 V	180		230	mA
			231		265	mA
Power at 1-dB Compression	P-1dB	V <sub>DS</sub> = 5 V; I <sub>DS</sub> = 50% I <sub>DSS</sub>	24	26		dBm
Power Gain at 1-dB Compression	G-1dB	V <sub>DS</sub> = 5 V; I <sub>DS</sub> = 50% I <sub>DSS</sub>	15.5	17		dB
Power-Added Efficiency	PAE	V <sub>DS</sub> = 5 V; I <sub>DS</sub> = 50% I <sub>DSS</sub> ; P <sub>IN</sub> = 10 dBm		55		%
Noise Figure	NF	V <sub>DS</sub> = 5 V; I <sub>DS</sub> = 50% I <sub>DSS</sub>		0.7		dB
Output Third-Order Intercept Point	IP3	V <sub>DS</sub> = 5 V; I <sub>DS</sub> = 50% I <sub>DSS</sub> ; P <sub>IN</sub> = -7 dBm		40		dBm
Maximum Drain-Source Current	I <sub>MAX</sub>	V <sub>DS</sub> = 2 V; V <sub>GS</sub> = 1 V		450		mA
Transconductance	G <sub>M</sub>	V <sub>DS</sub> = 2 V; V <sub>GS</sub> = 0 V	170	220		mS
Gate-Source Leakage Current	I <sub>GSO</sub>	V <sub>GS</sub> = -5 V		5	45	$\mu\text{A}$
Pinch-Off Voltage	V <sub>P</sub>	V <sub>DS</sub> = 2 V; I <sub>DS</sub> = 4 mA	-0.25	-1.2	-2.0	V
Gate-Source Breakdown Voltage Magnitude	V <sub>BDGS</sub>	I <sub>GS</sub> = 4 mA	-10	-12		V
Gate-Drain Breakdown Voltage Magnitude	V <sub>BDGD</sub>	I <sub>GD</sub> = 4 mA	-10	-13		V

frequency=1.8 GHz

- ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol	Test Conditions	Min	Max	Units
Drain-Source Voltage	$V_{DS}$	$T_{Ambient} = 22 \pm 3 \text{ }^{\circ}\text{C}$		7	V
Gate-Source Voltage	$V_{GS}$	$T_{Ambient} = 22 \pm 3 \text{ }^{\circ}\text{C}$		-3	V
Drain-Source Current	$I_{DS}$	$T_{Ambient} = 22 \pm 3 \text{ }^{\circ}\text{C}$		$I_{DSS}$	mA
Gate Current	$I_G$	$T_{Ambient} = 22 \pm 3 \text{ }^{\circ}\text{C}$		7.5	mA
RF Input Power	$P_{IN}$	$T_{Ambient} = 22 \pm 3 \text{ }^{\circ}\text{C}$		175	mW
Channel Operating Temperature	$T_{CH}$	$T_{Ambient} = 22 \pm 3 \text{ }^{\circ}\text{C}$		175	$^{\circ}\text{C}$
Storage Temperature	$T_{STG}$	—	-65	175	$^{\circ}\text{C}$
Total Power Dissipation	$P_{TOT}$	$T_{Ambient} = 22 \pm 3 \text{ }^{\circ}\text{C}$		1.75	W

Notes:

- Operating conditions that exceed the Absolute Maximum Ratings could result in permanent damage to the device.
- Power Dissipation defined as:  $P_{TOT} \equiv (P_{DC} + P_{IN}) - P_{OUT}$ , where  
 $P_{DC}$ : DC Bias Power  
 $P_{IN}$ : RF Input Power  
 $P_{OUT}$ : RF Output Power
- Absolute Maximum Power Dissipation to be de-rated as follows above 25 $^{\circ}\text{C}$ :  
 $P_{TOT} = 1.75\text{W} - (0.012\text{W}/^{\circ}\text{C}) \times T_{PACK}$   
 where  $T_{PACK}$  = source tab lead temperature
- This PHEMT is susceptible to damage from Electrostatic Discharge. Proper precautions should be used when handling these devices.

- OPTIMUM POWER OUTPUT MATCHING**

Frequency (GHz)	Load State	
	Magnitude	Phase
1.8	0.39	-168 $^{\circ}$
2.2	0.37	-147 $^{\circ}$
2.5	0.43	-135 $^{\circ}$

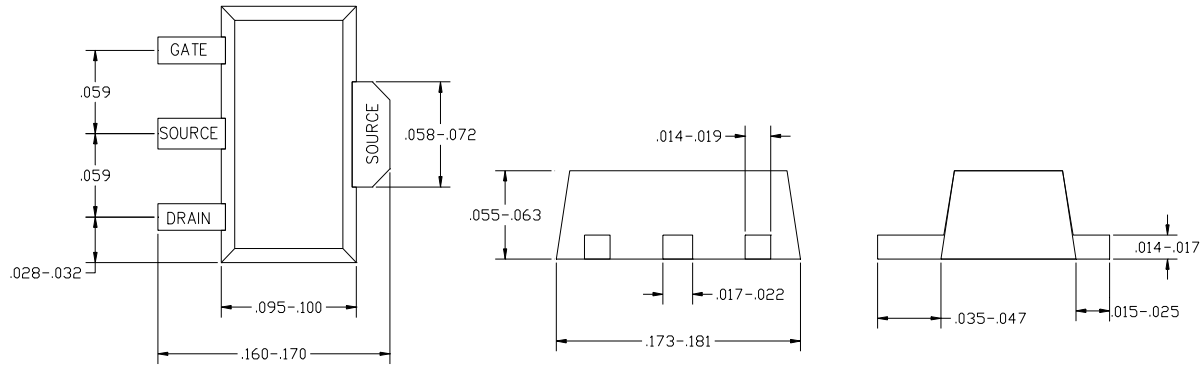
- HANDLING PRECAUTIONS**

To avoid damage to the devices care should be exercised during handling. Proper Electrostatic Discharge (ESD) precautions should be observed at all stages of storage, handling, assembly, and testing. These devices should be treated as Class 1A (0-500 V). Further information on ESD control measures can be found in MIL-STD-1686 and MIL-HDBK-263.

- APPLICATIONS NOTES & DESIGN DATA**

Applications Notes are available from your local Filtronic Sales Representative or directly from the factory. Complete design data, including S-parameters, noise data, and large-signal models are available on the Filtronic web site.

- **PACKAGE OUTLINE**  
(dimensions in inches)



All information and specifications are subject to change without notice.

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