PRELIMINARY DATA SHEET

SKY73201-364LF, SKY73202-364LF: Programmable 1–28 MHz 6th Order Low Pass Filters

Applications

- High-performance direct conversion receivers
- Software-defined radio basebands
- High-definition television tuners
- Medical imaging
- Flexible anti-aliasing and reconstruction filters

Features

- 6th order Butterworth low pass filter
- Exceptionally high dynamic range
- Auto-calibrated with clock reference, 20 MHz or 40 MHz nominal
- Programmable in steps from 1–28 MHz
- Nominal low pass filter step size of 1 MHz
- Single or dual channel configuration
- Serial bus control
- 5 x 5 mm QFN package
- Lead (Pb)-free, RoHS-compliant, and Green™, MSL-3 @ 260 °C per JEDEC J-STD-020

NEW

Skyworks Green™ products are RoHS (Restriction of Hazardous Substances)-compliant, conform to the EIA/EICTA/JEITA Joint Industry Guide (JIG) Level A guidelines, are halogen free according to IEC-61249-2-21, and contain <1,000 ppm antimony trioxide in polymeric materials.

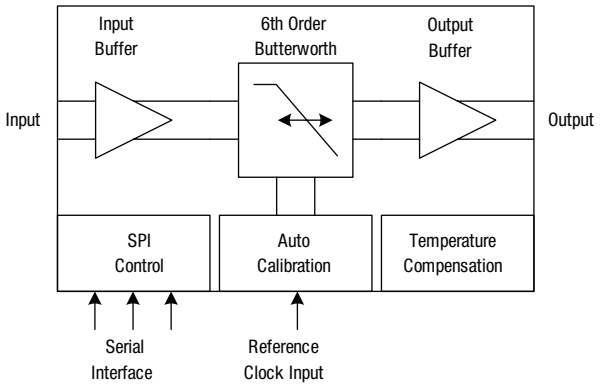
Description

The SKY73201-364LF & SKY73202-364LF are high-performance, programmable, monolithic, clock-referenced low-pass filters. They are configured as a 6th order Butterworth to provide extremely high stop-band isolation while maximizing pass-band flatness and minimizing group delay distortion. The corner frequency is programmable, via the 3-wire Serial Peripheral Interface (SPI), in steps, from 1–28 MHz, when a 20 MHz or 40 MHz reference is used. Nearly ideal Butterworth performance is maintained over temperature and process via a proprietary internal calibration circuit which derives its timing accuracy from the reference clock. Nominal reference clock frequencies of 20 MHz or 40 MHz are recommended to meet the specifications outlined in this data sheet but other reference clock frequencies can be accommodated with appropriate changes to the control register settings. The corner frequency range can be extended beyond 28 MHz by the use of alternate reference clock frequencies and modified control register settings. Please contact Skyworks Solutions applications engineering for assistance with your requirements.

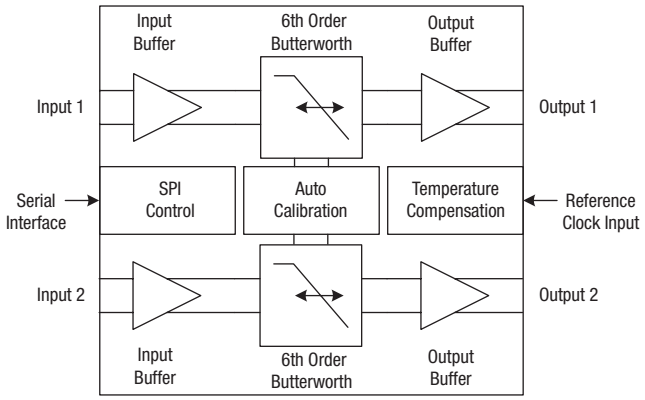
Additionally, the SKY73201-364LF & SKY73202-364LF offer excellent linearity and input noise level (83 dB SNR at 1 MHz corner setting), making them suitable for extremely high dynamic range applications such as adjacent channel rejection filters in direct conversion receivers. The I/O interface is fully differential, but may also be used single-ended, and on-chip input/output drivers allow easy integration between modern system components such as mixers, data converters, and variable gain amplifiers.

The dual configuration of SKY73202 offers the convenience of having two channels (such as the I and Q in vector demodulation) with closely matched characteristics that track each other. Both filters are programmed to the same settings by the common SPI interface.

SKY73201-364LF Functional Block Diagram



SKY73202-364LF Functional Block Diagram



Absolute Maximum Ratings

Characteristic	Value
Supply voltage	4.5 V
Supply current	100 mA
Signal input level	3 V_{PP}
Operating temperature	-40 °C to +85 °C
Storage temperature	-65 °C to +85 °C

Performance is guaranteed only under the conditions listed in the specifications table and is not guaranteed under the full range(s) described by the Absolute Maximum specifications. Exceeding any of the absolute maximum/minimum specifications may result in permanent damage to the device and will void the warranty.

CAUTION: *Although this device is designed to be as robust as possible, ESD (Electrostatic Discharge) can damage this device. This device must be protected at all times from ESD. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions must be employed at all times.*

Operating Characteristics

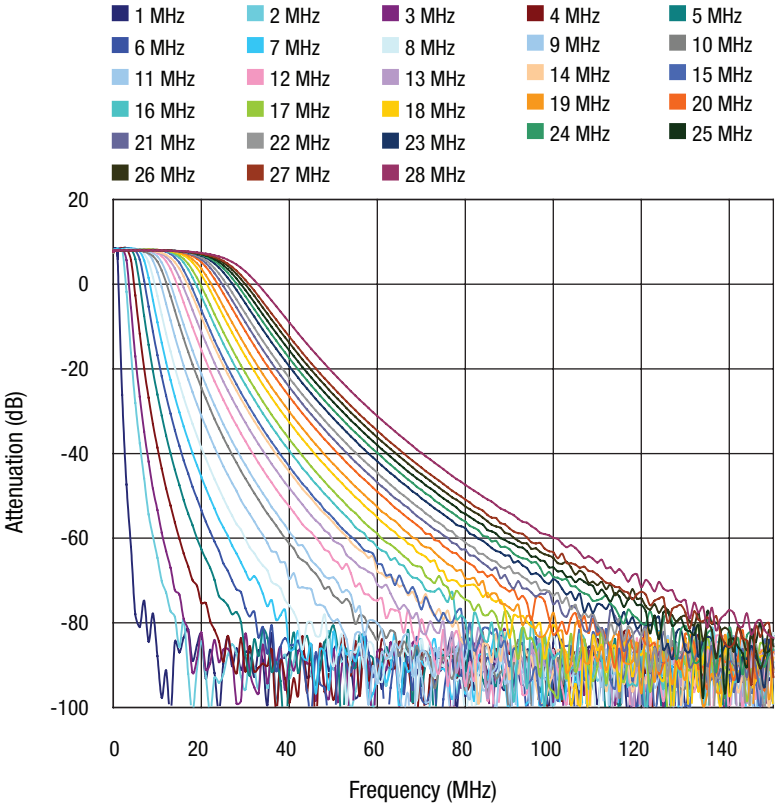
V_{DD} = 3.3 V, T = 25 °C, unless otherwise noted

Parameter	Condition	Frequency	Min.	Typ.	Max.	Unit
DC operating conditions						
Supply voltage			3	3.3	3.6	V
DC current	SKY73201-364LF SKY73202-364LF			32 59		mA mA
Signal performance						
Lowpass filter corner	6-pole Butterworth using an accurate 20 MHz or 40 MHz clock reference(4)		1		28	MHz
Lowpass filter step size				1		MHz
Lowpass corner frequency accuracy	Using an accurate 20 MHz or 40 MHz clock reference(4)			1	5	%
Lowpass rejection	Suppression at 2 X (3 dB corner frequency)			35		dB
Ultimate rejection level	Measured differentially			80		dB
Lowpass ripple	10 kHz to 0.8 X (3 dB corner frequency)			0.5	1	dB
Lowpass group delay variation(2)	For 10 MHz setting; from 10 kHz to 0.8 X (3 dB corner frequency)			35	44	ns
Lowpass group delay variation(2)	For 28 MHz setting; from 10 kHz to 0.8 X (3 dB corner frequency)			12	16	ns
Isolation	Between channel 1 and channel 2 (SKY73202) measured differentially			60		dB
Interface specifications						
Gain(1)	Selectable		0	6		dBv
Input load	Differential		10kII 2			ΩII pF
Input-referred noise	At 6 dB gain setting			25		nV/ Hz
Input common mode voltage range			0.8		2.5	V
Input 1 dB compression	0 dB gain setting		1.2			V D_{PP}
Input SNR	At 1 MHz corner setting		80	83		dB
Output drive capability(3)	Differential		1000	5000		
Output load capacitance					15	pF
Common-mode voltage			1.35	1.50	1.70	V
Output linear signal swing	1 dB compression level; differential		1.2	2.0		V D_{PP}

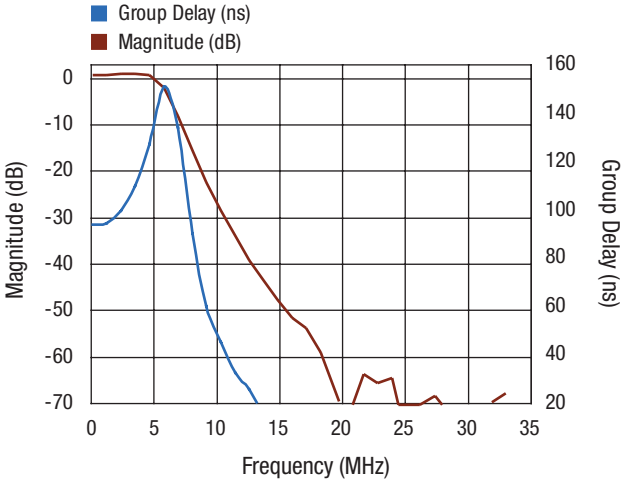
1. Gain in dBV = $20\log_{10}$ (V_{OUT_RMS}/V_{IN_RMS}), independent of impedance.
2. Group delay scales inverse-linearly with cutoff frequency; average group delay variation = 350 ns/Cutoff_in_MHz
3. A 50 + 50 Ω load may be driven but voltage gain may be reduced and signal-linearity may be affected. The overall filter shape should be preserved.
4. The reference clock signal must have a duty cycle of 50%.

Typical Performance Data

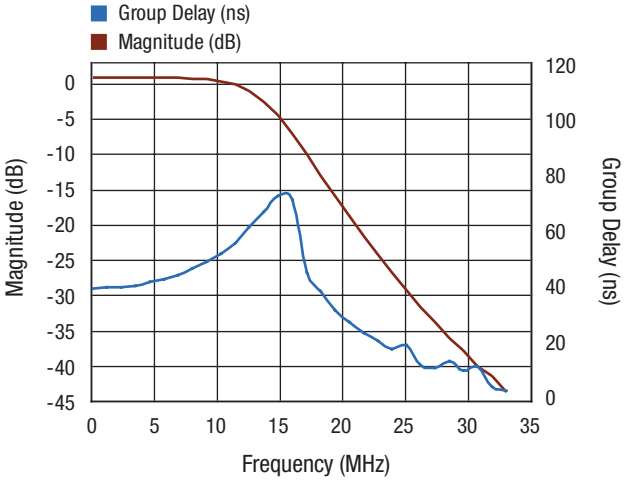
V_{DD} = 3.3 V, T = 25 °C, unless otherwise noted



Programmable Filter Amplitude Response

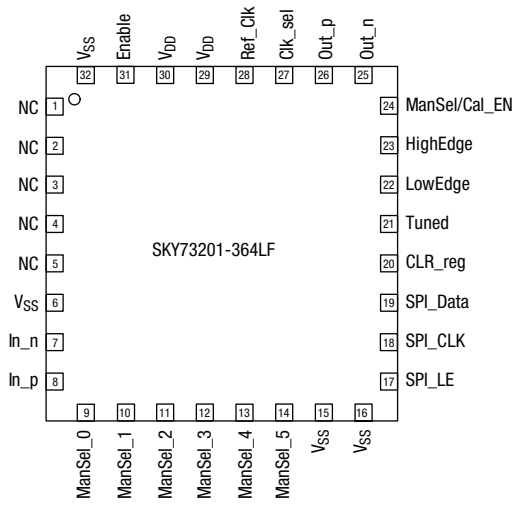


Filter Response with 3 dB Cutoff Tuned to 8 MHz



Filter Response with 3 dB Cutoff Tuned to 14 MHz

SKY73201-364LF Pin Out Diagram

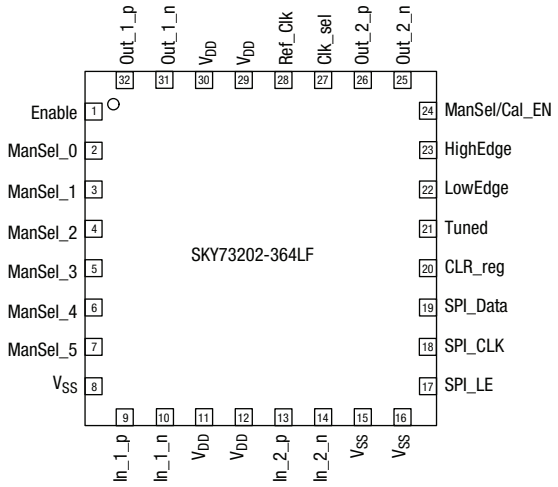


SKY73201-364LF Pin Descriptions

Pin #	Name	Description
1	N/C	No connection
2	N/C	No connection
3	N/C	No connection
4	N/C	No connection
5	N/C	No connection
6	V_{SS}	Ground
7	In_n	Filter input -
8	In_p	Filter input +
9	ManSel_0	Connect to GND in auto tuning mode(1)
10	ManSel_1	Connect to GND in auto tuning mode(1)
11	ManSel_2	Connect to GND in auto tuning mode(1)
12	ManSel_3	Connect to GND in auto tuning mode(1)
13	ManSel_4	Connect to GND in auto tuning mode(1)
14	ManSel_5	Connect to GND in auto tuning mode(1)
15	V_{SS}	Ground
16	V_{SS}	Ground
17	SPI_LE	SPI latch enable (see timing diagram)
18	SPI_CLK	SPI clock Input
19	SPI_DATA	SPI serial data (bi-directional I/O)
20	CLR_reg	Normally set LOW; set HIGH to clear all registers to zero
21	Tuned	Filter tuned indication; HIGH when filter is settled
22	LowEdge	No connect (filter settle error indicator, debug only)
23	HighEdge	No connect (filter settle error indicator, debug only)
24	ManSel/Cal_EN	Manual mode enable/calibration enable; Held HIGH for manual mode(1). In automatic mode, it is normally LOW but must be toggled HIGH then LOW to start/reset the autocal circuit (see timing diagram)
25	Out_n	Filter output -
26	Out_p	Filter output +
27	Clk_sel	Reference clock select; connect to V_{DD} if Ref_Clk is 40 MHz, connect to V_{SS} if Ref_Clk is 20 MHz
28	Ref_Clk	Reference clock; selectable 20 or 40 MHz (needed during calibration only)
29	V_{DD}	Power supply (+3.3 V_{DC})
30	V_{DD}	Power supply (+3.3 V_{DC})
31	ENABLE	Chip enable; chip is enabled when HIGH (V_{DD}), standby mode when LOW (V_{SS})
32	V_{SS}	Ground (GND)
Paddle		Must be connected via lowest possible impedance to ground for proper electrical and thermal performance

1. The manual select pins are for manual fine tuning of the filter corner frequency. Normally these inputs are grounded since tuning is performed by the automatic calibration circuit operating with the reference clock. If the "ManSel" pin (24) is set high, then pins 9-14 would be active to perform fine tuning by the user (but in this case auto cal would not be operational and the filter would not be clock referenced).

SKY73202-364LF Pin Out Diagram



SKY73202-364LF Pin Descriptions

Pin #	Name	Description
1	ENABLE	Chip enable; chip is enabled when HIGH (V_{DD}), standby mode when LOW (V_{SS})
2	ManSel_0	Connect to GND in auto tuning mode(1)
3	ManSel_1	Connect to GND in auto tuning mode(1)
4	ManSel_2	Connect to GND in auto tuning mode(1)
5	ManSel_3	Connect to GND in auto tuning mode(1)
6	ManSel_4	Connect to GND in auto tuning mode(1)
7	ManSel_5	Connect to GND in auto tuning mode(1)
8	V_{SS}	Ground
9	In_1_p	Filter No. 1 input +
10	In_1_n	Filter No. 1 input -
11	V_{DD}	Power supply (+3.3 V_{DC})
12	V_{DD}	Power supply (+3.3 V_{DC})
13	In_2_p	Filter No. 2 input +
14	In_2_n	Filter No. 2 input -
15	V_{SS}	Ground
16	V_{SS}	Ground
17	SPI_LE	SPI latch enable (see timing diagram)
18	SPI_CLK	SPI clock Input
19	SPI_DATA	SPI serial data (bi-directional I/O)
20	CLR_reg	Normally set LOW; set HIGH to clear all registers to zero
21	Tuned	Filter tuned indication; HIGH when filter is settled
22	LowEdge	No connect (filter settle error indicator, debug only)
23	HighEdge	No connect (filter settle error indicator, debug only)
24	ManSel/Cal_EN	Manual Mode Enable/ Calibration Enable; Held HIGH for manual mode(1). In automatic mode, it is normally LOW but must be toggled HIGH then LOW to start/reset the AutoCal circuit (see timing diagram)
25	Out_2_n	Filter No. 2 output -
26	Out_2_p	Filter No. 2 output +
27	Clk_sel	Reference clock select; connect to V_{DD} if Ref_Clk is 40 MHz, connect to V_{SS} if Ref_Clk is 20 MHz
28	Ref_Clk	Reference clock; selectable 20 or 40 MHz (needed during calibration only)
29	V_{DD}	Power supply (+3.3 V_{DC})
30	V_{DD}	Power supply (+3.3 V_{DC})
31	Out_1_n	Filter No. 1 output -
32	Out_1_p	Filter No. 1 output +
Paddle		Must be connected via lowest possible impedance to ground for proper electrical and thermal performance

1. The manual select pins are for manual fine tuning of the filter corner frequency. Normally these inputs are grounded since tuning is performed by the automatic calibration circuit operating with the reference clock. If the "ManSel" pin (24) is set high, then pins 9–14 would be active to perform fine tuning by the user (but in this case auto cal would not be operational and the filter would not be clock referenced).

Serial I/O Interface Information

The primary control interface is a three-wire bidirectional serial interface. The interface operates as slowly as DC, and as fast as 100 Mbps. The three interface signals are SPI_CLK, SPI_DATA and SPI_LE. The serial data bits are latched into the serial interface on each rising edge of SPI_CLK. Data is latched into the target register by the rising edge of SPI_LE. There are 3 functional data registers, each containing 8 data bits. Each register is independent and can be read or written in any order.

Each serial interface transaction, read/write, consists of 16 bits: 1 start bit, 2 reserved bits (0s), 1 read/write bit, 4 address bits followed by 8 data bits. See Figure 1.

ADDRESS Byte

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Start bit = 1	Reserved = 0	Reserved = 0	Read/ write	A3	A2	A1	A0

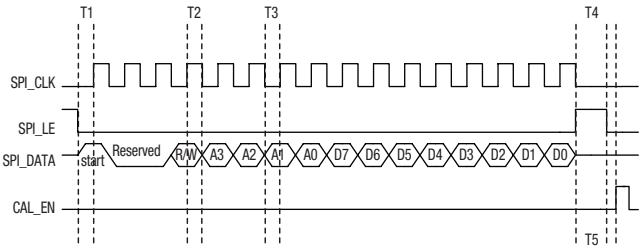
DATA Byte

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
D7	D6	D5	D4	D3	D2	D1	D0

Figure 1. SPI Transaction Bit Definitions

The setup and hold timing requirements are shown in Figure 2 and the SPI Interface Timing Requirements table. The SPI_LE line must have a setup time of (T1) before the first clock edge. All data bits must be held for a minimum of (T2) after the rising clock edge. The minimum setup time for any bit edge is (T3) before the rising edge of SPI_CLK. The SPI_LE signal must be held for a minimum time (T4) between transactions and held high when other SPI devices on the bus are active. The CalEn signal must be toggled after all the register configuration is complete in order to initiate the auto calibration feature. The configuration of all the registers will require approximately 50 SPI_CLK cycles and the auto calibration will require approximately 50 Ref_Clk cycles. The TUNED pin will go high at the successful completion of auto calibration and may be used to disable the reference clock source.

On power up, all registers will be cleared to 0 and the filter's inputs and outputs will be in an isolated state. All registers retain their data when ENABLE is held to the standby state, ground. In this condition the filter inputs and outputs will be in an isolated state. When ENABLE is taken to V_{DD}, inputs and outputs will be in an isolated state until CalEn is toggled and auto calibration has completed.



Register read back is optional and is not required for normal function.
*R/W Bit Sets Direction of Data Line for Serial Read-back; Read = 0, Write = 1.
** Cal_EN Line is toggled AFTER ALL registers are written.

Figure 2. SPI Register Configuration Timing Diagram

SPI Interface Timing Requirements

Parameter	Description	Min	Unit
T1	Setup time LE to DATA	5	ns
T2	Hold time CLK to DATA	5	ns
T3	Setup time DATA to CLK	5	ns
T4	LE Width	10	ns
T5	LE to CalEn	10	ns

SPI Register Map Detail

SKY73201 & SKY73202 Configuration Register Map

Address	Bit Field	Register Name	Usage
0	[2:0]	ResSkewCtr	Corner frequency fine tune
	[7:3]	ResDacCtr	Calibration constant
1	[4:0]	ResCtr	Calibration constant
	[6:5]	BandSel	Sets filter corner frequency
	[7]	Reserved	Write to zero
2	[4:0]	GainCtr	Sets filter gain
	[7:5]	Reserved	Write to zero

6 dB Gain Configuration Register Lookup Table

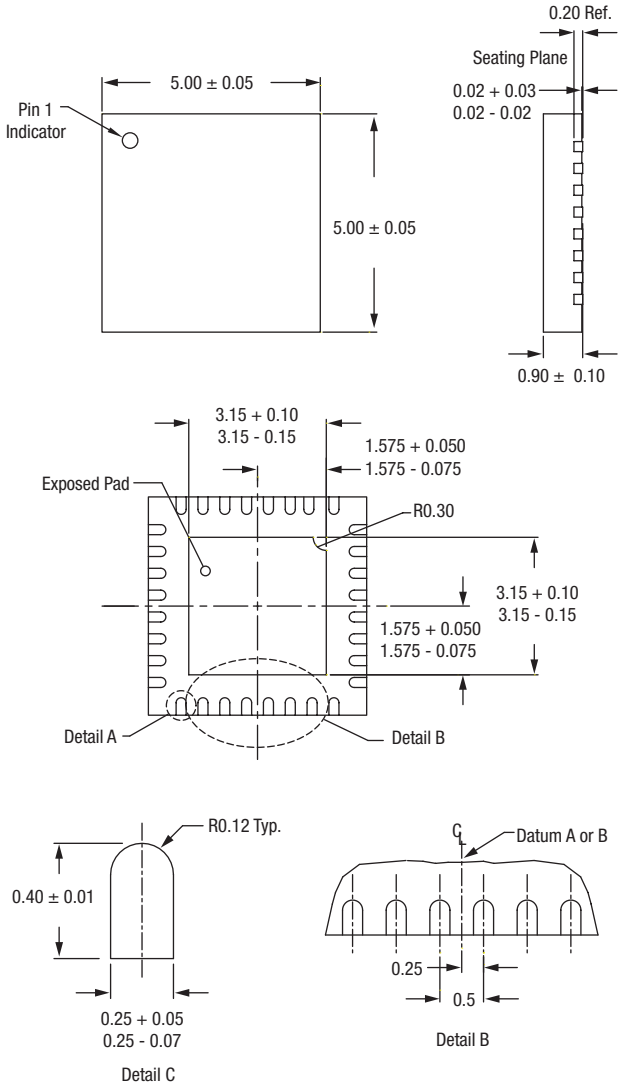
3 dB Cutoff (MHz)	Address 0 (Hex)	Address 1 (Hex)	Address 2 (Hex)
1	0F	01	01
2	17	02	02
3	1F	03	03
4	27	04	04
5	2F	05	05
6	37	06	06
7	3F	07	07
8	47	08	08
9	4F	09	09
10	57	0A	0A
11	64	0C	0C
12	6C	0D	0D
13	75	0E	0E
14	7D	0F	0F
15	80	10	10
16	88	11	11
17	90	12	12
18	A4	14	14
19	AC	15	15
20	B5	16	16
21	BD	17	17
22	C5	18	18
23	CD	19	19
24	DC	1A	1A
25	E4	1B	1B
26	EC	1C	1C
27	F4	1D	1D
28	F0	1E	1E
660 kHz (uncalibrated)	10	62	02
330 kHz (uncalibrated)	08	61	01

0 dB Gain Configuration Register Lookup Table

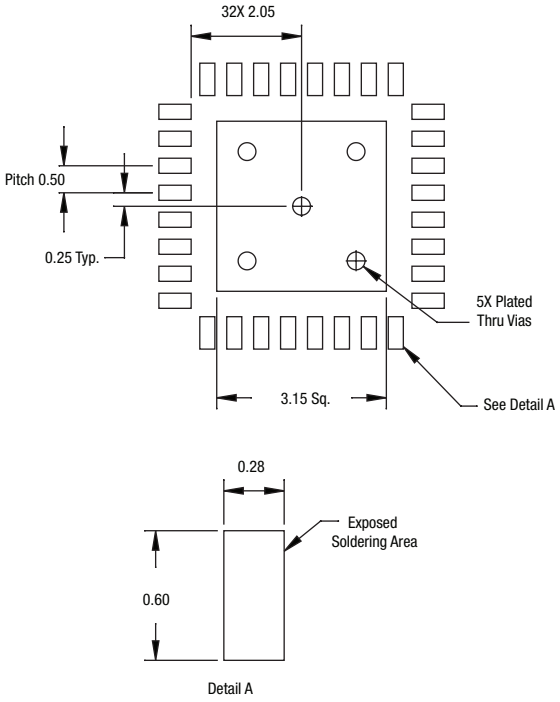
3 dB Cutoff (MHz)	Address 0 (Hex)	Address 1 (Hex)	Address 2 (Hex)
1	0F	01	01[1]
2	17	02	01
3	1F	03	01[1]
4	27	04	02
5	2F	05	02[1]
6	37	06	03
7	3F	07	03[1]
8	47	08	04
9	4F	09	04
10	57	0A	05
11	64	0C	06
12	6C	0D	07
13	75	0E	07
14	7D	0F	08
15	80	10	08
16	88	11	08
17	90	12	09
18	A4	14	0A
19	AC	15	0B
20	B5	16	0B
21	BD	17	0C
22	C5	18	0C
23	CD	19	0D
24	DC	1A	0D
25	E4	1B	0E
26	EC	1C	0E
27	F4	1D	0F
28	F0	1E	0F
660 kHz (uncalibrated)	10	62	01
330 kHz (uncalibrated)	08	61	01[1]

1. This value will give the closest available gain setting. The resulting gain will not meet overall specification. Please test for application suitability.

QFN 5 x 5 (-364)



Land Pattern



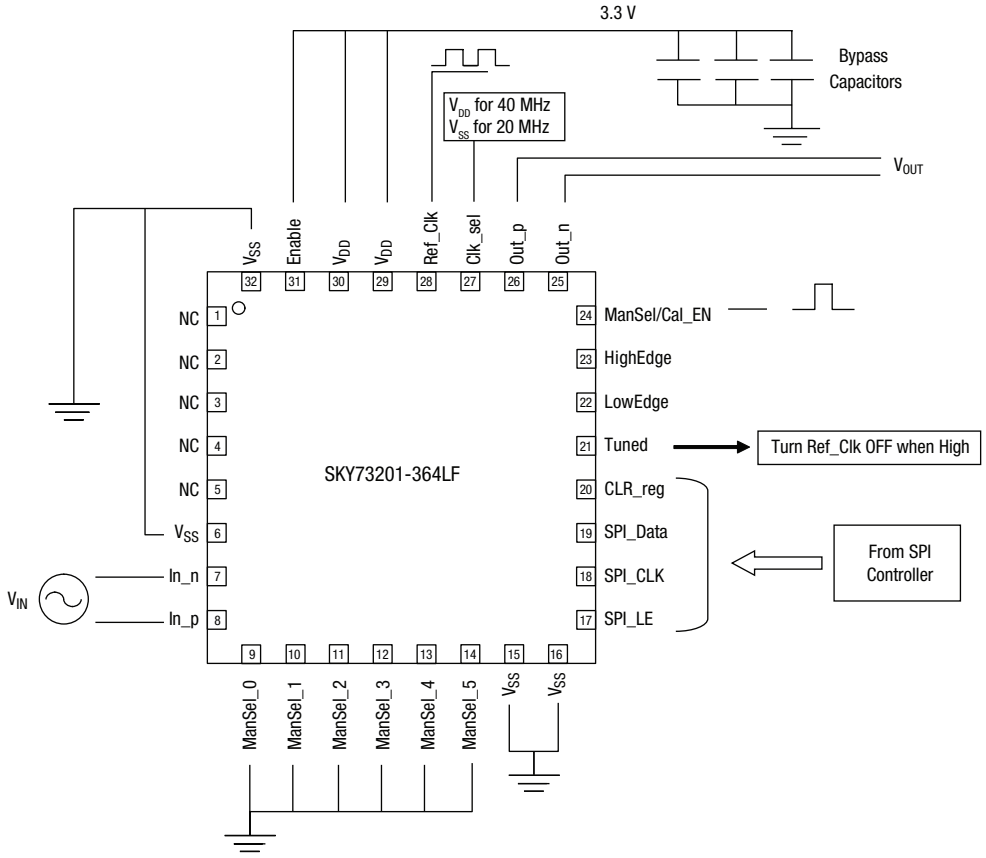
Recommended Solder Reflow Profiles

Refer to the *"Recommended Solder Reflow Profile"* Application Note.

Tape and Reel Information

Refer to the *"Discrete Devices and IC Switch/Attenuators Tape and Reel Package Orientation"* Application Note.

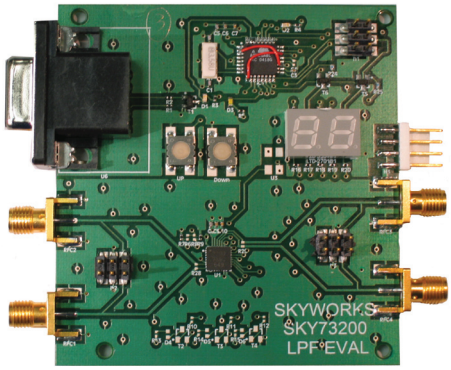
Basic Application Diagram



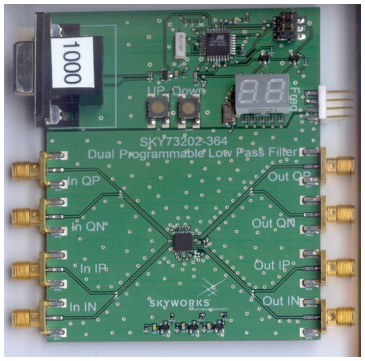
Evaluation Board Description

Evaluation boards for the SKY73201 and SKY73202 support both stand-alone evaluation and automated evaluation via the use of personal computer (PC) software to control the configuration of the filters through the PC's serial port. The onboard microcontroller configures the filter based on input from either the onboard pair of push buttons in stand-alone mode or from the serial port in automated mode. In the automated mode, all of the control parameters can be set to any valid register value, allowing evaluation over the full performance range. In stand-alone mode the 2 digit display will accurately display the selected corner frequency. There is an onboard oscillator (X1) to provide the clock for the micro controller and a separate oscillator (U3) as the filter's reference clock. Three LEDs are provided to indicate the current state of the filter's auto calibration feature.

Evaluation Board (With On-Board Micro-Controller)

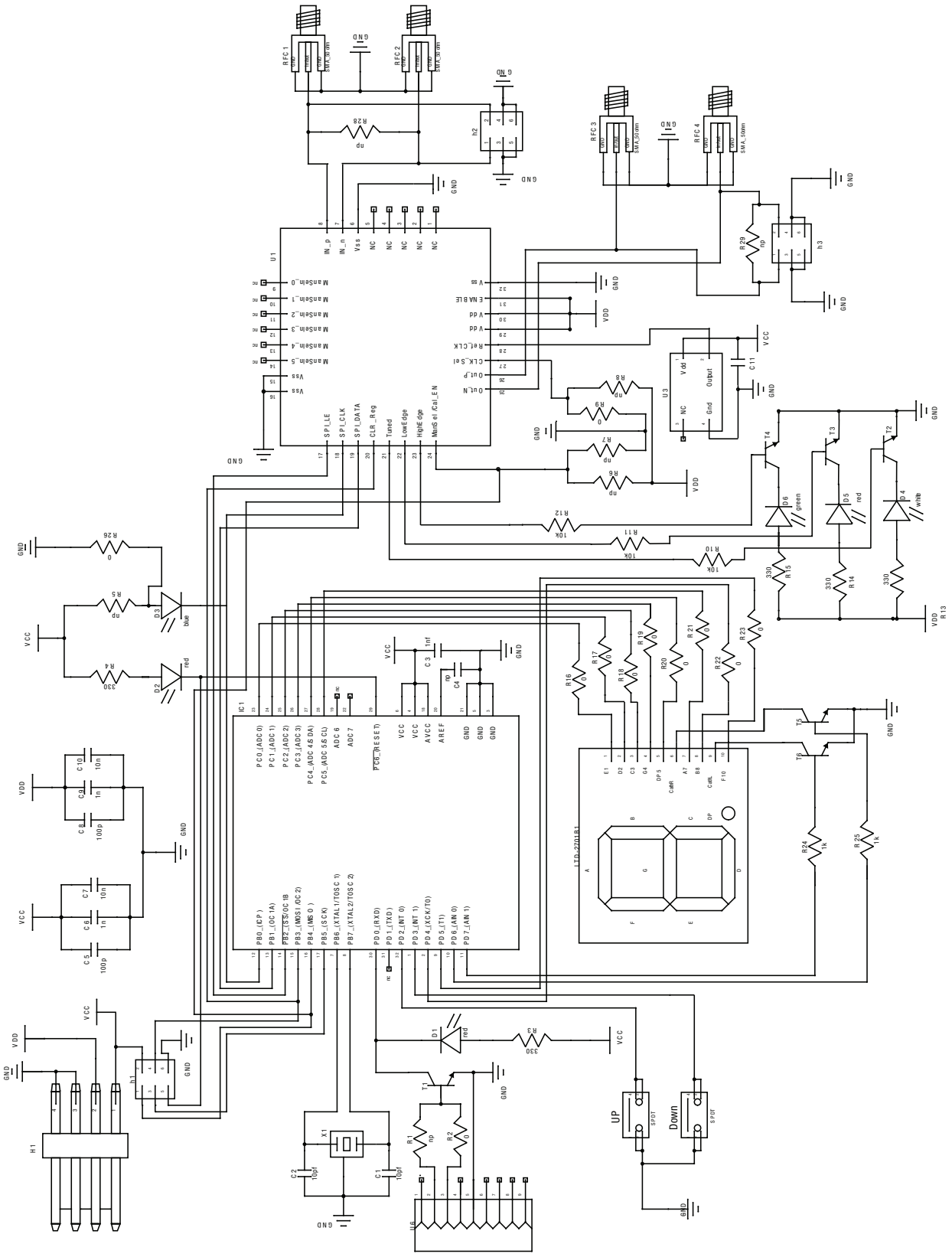


SKY73201

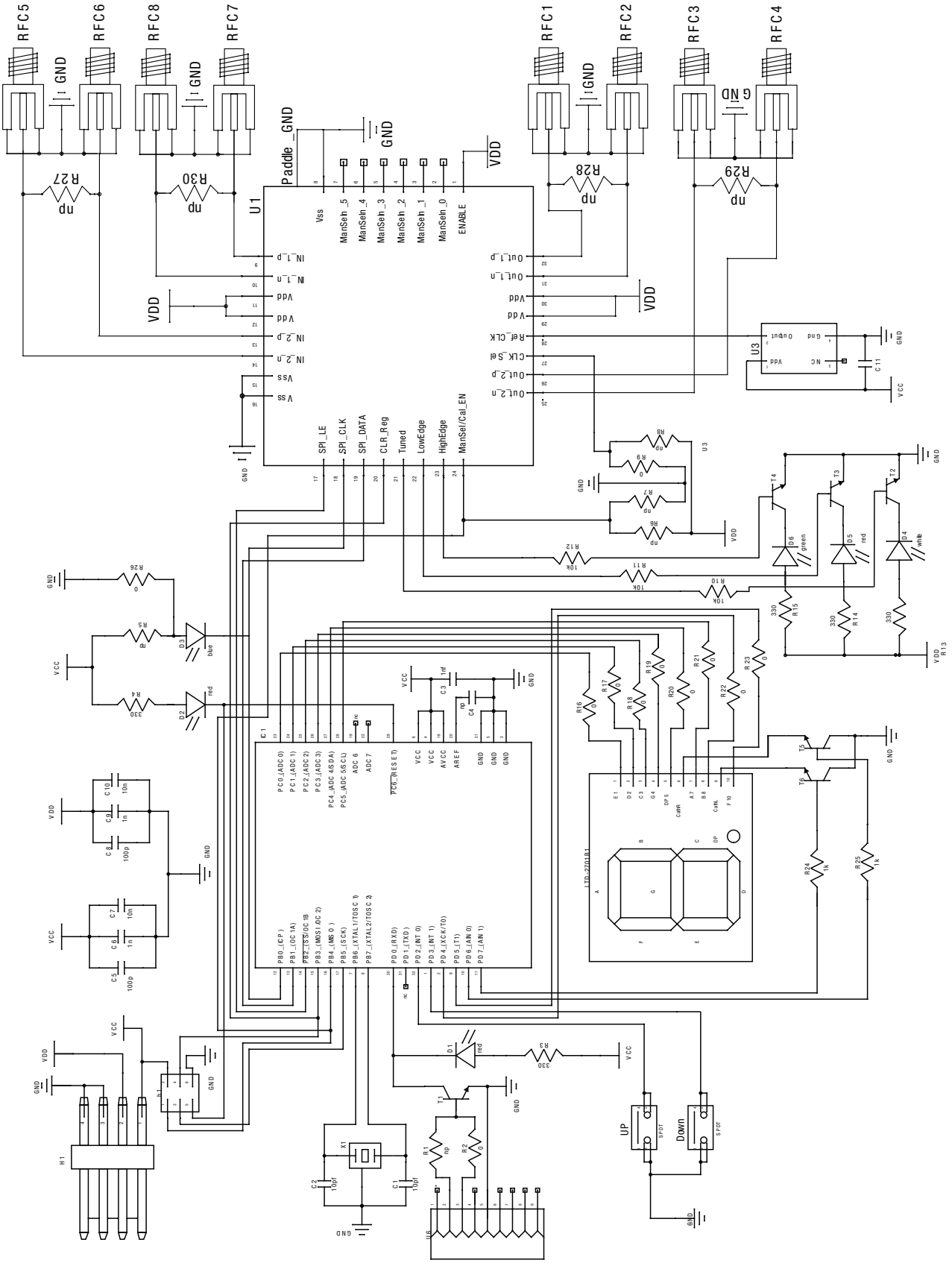


SKY73202

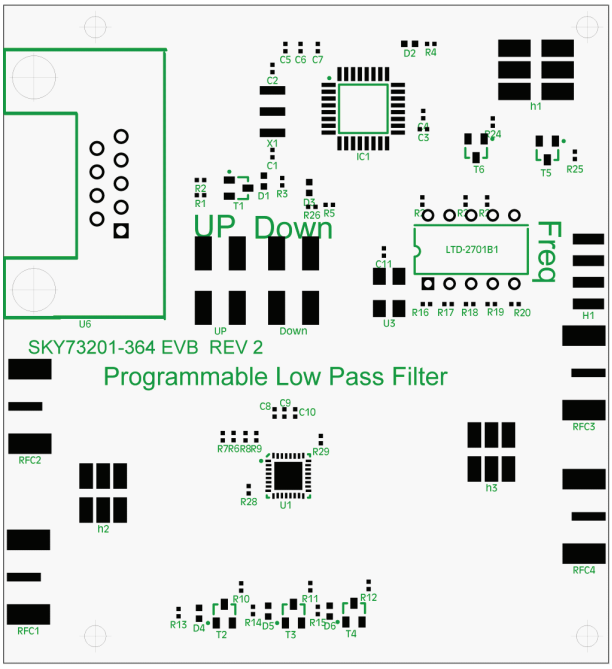
SKY73201 Evaluation Board Schematic



SKY73202 Evaluation Board Schematic

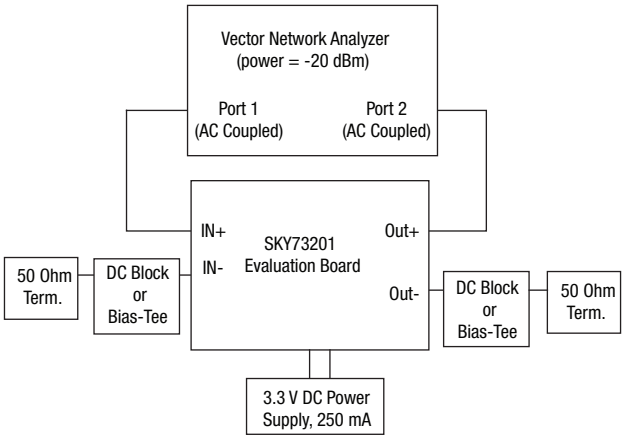


SKY73201 Evaluation Board Assembly Drawing



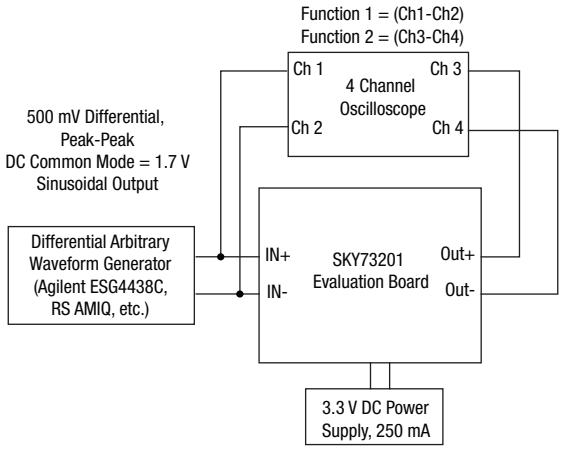
Single-Ended Test Configuration

This setup uses conventional RF test equipment (RF signal generator and spectrum analyzer may be used instead of VNA).



Note: DC blocks and terminations are placed on unused differential ports.

Fully Differential Test Configuration



Application Notes

All current application notes are available on the web at http://www.skyworksinc.com

Evaluation Boards

Evaluation boards for the SKY73201 and SKY73202 support both stand-alone evaluation and automated evaluation via the use of personal computer (PC) software to control the configuration of the filters through the PC's serial port. The onboard microcontroller configures the filter based on input from either the onboard pair of push buttons in stand-alone mode or from the serial port in automated mode. In the automated mode, all of the control parameters can be set to any valid register value, allowing evaluation over the full performance range. In stand-alone mode the 2-digit display will accurately display the corner frequency setting. There is an onboard oscillator (X1) to provide the clock for the micro controller and a separate oscillator (U3) to provide the filter's reference clock. Three LEDs are provided to indicate the current state of the filter's auto calibration feature.

On the evaluation boards, the reference clock and the microcontroller clock are active continuously and can be potential noise sources. In applications demanding high signal purity, these potential noise sources can be eliminated after the configuration and auto calibration are completed. To test the device without the reference clock, microcontroller, microcontroller clock and display operating, the following procedure is recommended:

1) Remove the soldered-in-wire jumper between pins #1 and #2 of the DC power connector H1.
2) Connect a 3.3 V supply to pin #1 of H1 to power the microcontroller and the clock sources and connect a second independent 3.3 V supply to pin #2 of H1 to power only the filter.
3) With both supplies enabled, set the configuration registers as required. Once the auto calibration has completed, the white LED (D4) will illuminate, indicating that the filter is tuned.
4) Disable the power supply connected to pin #1. This will disable everything on the evaluation board except the filter, which will hold the correct tuned state.
5) In this configuration, any possible spurs due to clock signals are eliminated.

Programming and Calibration Procedure and Intervals

Register configuration time: This operation requires a minimum of 50 SPI clock cycles to write all three configuration registers. The fastest supported SPI clock speed is 100 MHz, which will result in a minimum configuration time of 500 ns.

Automatic calibration: After all of the registers have been written, the Cal_EN pin must be toggled (i.e. raised high and then low). The auto calibration starts on the negative edge of Cal_EN.

During this process, the reference clock (nominally 20 MHz) must be present to provide the timing information. The calibration process may take up to 50 reference clock cycles. When calibration is complete, the "Tuned" pin will go high, indicating that the calibration has successfully completed. The output of the "Tuned" pin may be used to gate off the reference clock as it is not required for standard operation. This is preferred in applications where possible spurs related to the clock and its harmonics may cause undesired degradation of the signal.

For devices used in the auto tuning mode only, the ManSel_0 through ManSel_5 pins should be grounded (not left floating).

Setup time: If both the SPI clock and reference clock are selected to be 20 MHz, the entire filter corner frequency configuration & calibration procedure may take up to 5 µs (corresponding to 50 + 50 = 100 clock cycles).

Manual calibration: After the registers are configured, the device may also be calibrated (fine-tuned) manually through the use of the ManSel/CalEn pins. Manual tuning mode is enabled by holding the ManSel pin high. This allows the ManSel_0 through ManSel/CalEn_5 pins to operate as a 6-bit parallel bus whose binary value adjusts the cutoff frequency of the filter. For more details on this mode of operation, please consult Skyworks.

General Layout Recommendations:

1) Keep all analog traces differential (equal length, no ground in between)
2) Place multiple vias on the outside of the differential pairs (but not between the differential lines)
3) Route all other traces perpendicularly across the differential pair, and never between the analog lines and their ground reference
4) Locate all decoupling capacitors as close to the device as possible, Place multiple ground vias on the capacitors
5) Place as many ground vias under the filter paddle as possible.

Reference Clock Selection

For best filter corner frequency accuracy, a crystal-based clock (as opposed to ceramic), with an accuracy better than 1000 ppm over temperature, aging, and process is recommended. The clock input to the SKY73201/2 is CMOS logic (threshold approx. 1.7 V) so most clocks that operate on a 3.3 V supply should be compatible. In addition, the duty cycle of the clock affects filter corner accuracy. The closer the duty cycle is to 50%, the more accurate the filter corner setting. The nominal clock frequencies are 20 MHz, with CLK_Sel tied to ground, or 40 MHz with CLK_Sel tied to V_{DD}. Alternate reference clock frequencies in a range of ±20% can usually be accommodated with appropriate changes to the configuration register values. Alternate reference clock frequencies may also allow a wider range of corner frequencies of approximately ±20% with appropriate changes to the configuration register values.

Output Drive Capability

The SKY73201 and SKY73202 have op-amp based output drivers, whose effective source impedance is in the few 10's of ohms range and a current drive capability of approximately 2–3 mA. While it is intended to drive a high impedance data converter or a PGA, it can also drive a 100 Ω differential load (or a 50 Ω single-ended load) at a reduced gain level. As long as the output voltage swing required does not push the output drivers into current clipping, the filter shape will be maintained at a reduced gain. Please note that the gain values that are specified in the datasheet are based on the specified, high, input and output impedances.

Filter Gain Setting

The SKY73201 and SKY73202 allow approximately 6 dB of adjustment over gain in addition to the ability to set the 3 dB cutoff frequency for fine-tuning the filter gain.

The gain may be controlled by adjusting the GainCtr register value, Address2[4:0]. The gain is a linear ratio expressed in terms of the GainCtr register value and the ResCtr register value, Address1[4:0], that sets the filter cut-off frequency

$$\text{Gain} = 2 \bullet \frac{\text{Address2<4:0>}}{\text{Address1<4:0>}} = 2 \bullet \frac{\text{GainCtr}}{\text{ResCtr}}$$

Note: For the linear gain calculation, please use the decimal equivalents of the binary representations in the above ratio.

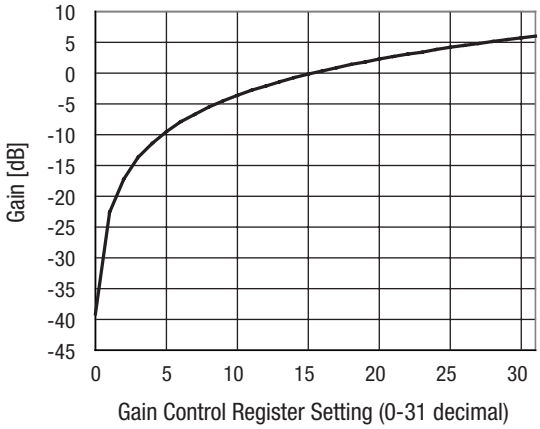
The configuration procedure involve determining the appropriate values for the desired corner frequency (from register configuration tables) and then modifying the GainCtr value in register Address2[4:0] for the desired gain.

Example (For a 14 MHz filter corner setting):

Gain Adjustment Example

Gain	Address0	Address1	Address2
6 dB	7D	0F	0E
3 dB	7D	0F	0B
0 dB	7D	0F	08

As an example, the effect of the GainCtr register value, Address 2[4:0], for the 28 MHz corner setting is shown in the plot below. The 0 setting corresponds to open circuit and decimal 31 setting corresponds to maximum gain.



SKY73201 Gain vs. Register Setting

Input and Output Interface and Common-Mode Voltage

At the input, the common-mode voltage must be supplied by the device driving the filter. At the output, the filter biases itself to a common-mode voltage that is approximately half of the V_{DD}. (e.g. 3.3*1/2 = 1.65 V). The output common-mode voltage setting is independent of the input common-mode voltage. Only the differential component of the input signal will pass through the filter.

The device requires a minimum of 1 kΩ load (500 Ω each arm) in order to maintain full gain performance. This accommodates a majority of available data converters.

If the device immediately before the programmable filter has a different common-mode voltage (e.g. 3.5 V from a 5 V device), then a matching network may be used to convert the 3.5 V offset to 1.65 V. This may be done with two series resistors into the + and – arms and a shunt resistor between the two. (Shunt resistor value on the order of 1kΩ). Careful selection of the values of the resistors is required so as to not add extra noise at the input and degrade the input referred noise of the device. (The input referred noise is specified assuming 1–2 kΩ input loading resistors.)

Single-Ended to Differential Configuration

To use the programmable filter with a single-ended input signal and a differential output signal, simply apply the single-ended input signal to one of the input ports and apply a DC midpoint voltage (equal to the average level of the signal) to the other input port.

Interfacing to the SKY73201 and SKY73202 Filters

Figure 3 shows a simplified schematic of the inputs to the SKY73201 filter. The input stage is a 2-stage op-amp with bipolar transistor input, which implies that the preceding stage must supply the base current and a common-mode voltage. A common-mode base voltage of 1.65 V should be applied to the inputs. Any external resistance in series with pins 7 and 8 will reduce the gain of the filter. (The same recommendations apply to the inputs of the SKY73202 filter.)

Figure 4 shows a simplified schematic of the output buffer of the SKY73201. The device generates a common-mode voltage of 1.65 V at the output and the output buffers are designed to drive a minimum of 5 kΩ impedance. If the device is loaded with a resistance lower than 5 kΩ, it will cause loss in signal swing, which may reduce the gain and affect the signal linearity. (The same recommendations apply to the SKY73202 filter.)

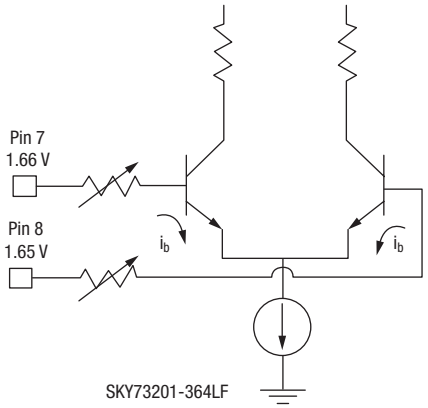


Figure 3. Simplified Schematic of Input

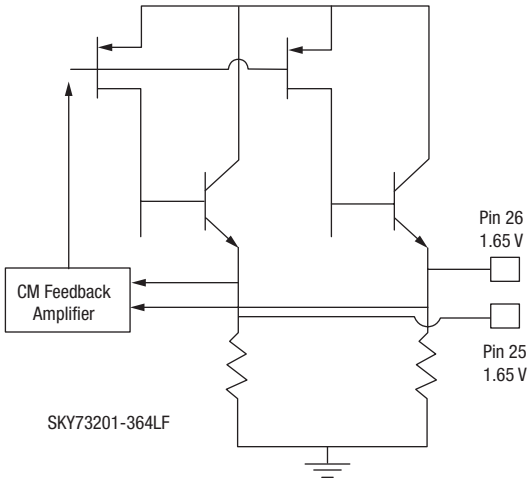


Figure 4. Simplified Schematic of the Filter Output

Output common-mode compensation

If the stage following the SKY73201 or SKY73202 requires a common-mode voltage that is lower or higher than 1.65 V, the new common-mode voltage can be established by simple resistive voltage division. Figure 5 shows a simple application circuit in which the SKY73201 filter is used to drive a 1.8 V data converter with an input common-mode voltage of 0.9 V.

It is important to design adequate supply bypassing by means of bypassing capacitors as any noise coupled into the device may affect the corner frequency accuracy. The exact values of the bypass capacitors will depend on the application environment.

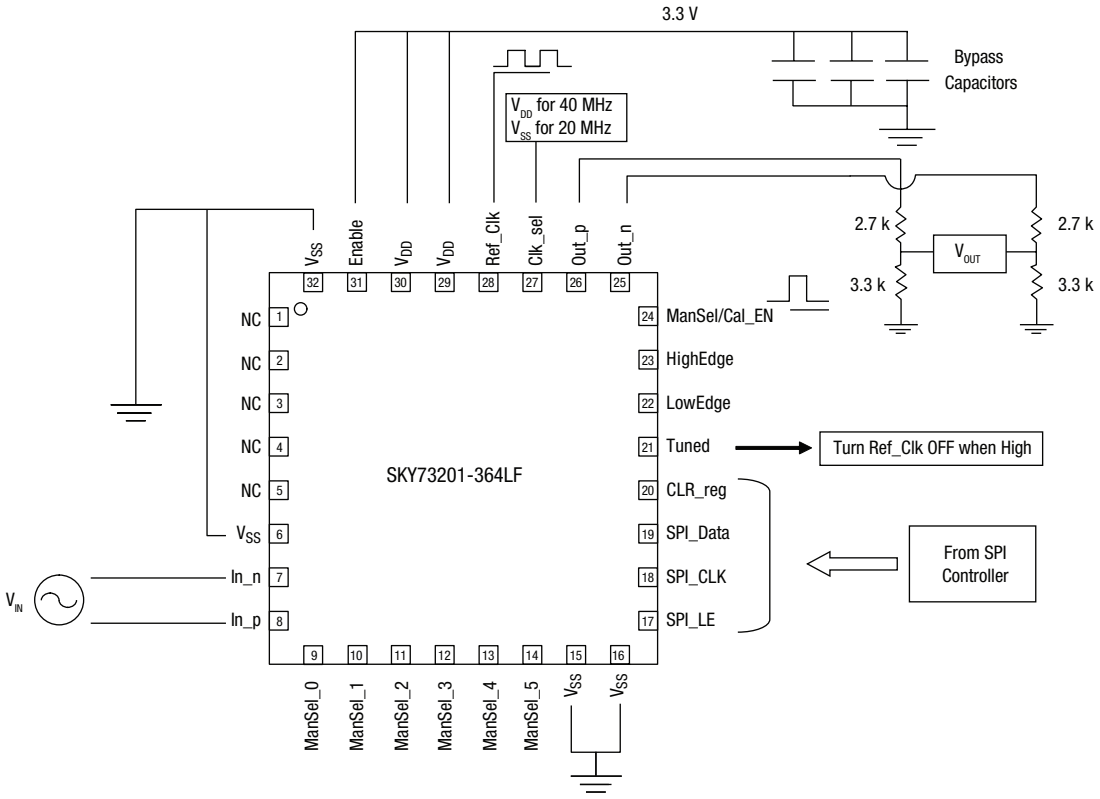


Figure 5. SKY73201 Application Circuit with 0.9 V Output Common-mode Voltage