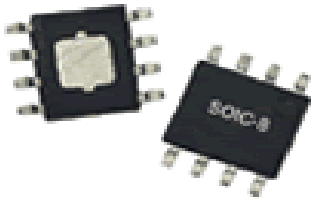
AH312-S8G

2 Watt, High Linearity InGaP HBT Amplifier

Applications

- Final stage amplifiers for Repeaters
- Mobile Infrastructure
- Driver stage for High Power Amplifier
- LTE / WCDMA / EDGE / CDMA

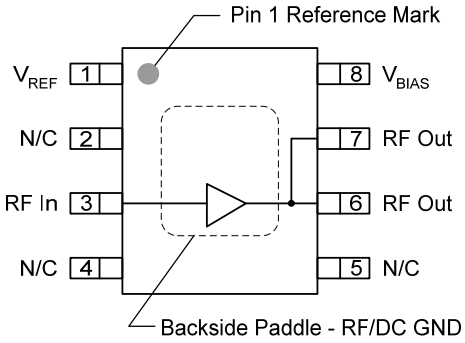


SOIC-8 Package

Product Features

- 400–2300 MHz
- +33 dBm P1dB at 2140 MHz
- +48 dBm Output IP3 at 2140 MHz
- 18 dB Gain at 900 MHz
- +5 V Single Positive Supply
- MTTF > 100 Years
- Lead-free/RoHS-compliant SOIC-8 SMT Package

Functional Block Diagram



General Description

The AH312-8SG is a high dynamic range driver amplifier in a low-cost surface mount package. The InGaP/GaAs HBT is able to achieve high performance for various narrowband-tuned application circuits with up to +49 dBm OIP3 and +33 dBm of compressed 1dB power. It is housed in a lead-free/RoHS-compliant SOIC-8 package. All devices are 100% RF and DC tested.

The AH312-8SG is targeted for use as a driver amplifier in wireless infrastructure where high linearity and medium power is required.

An internal active bias allows the AH312-8SG to operate directly off a single +5 V supply and maintain high linearity over temperature. These operational features make the AH312-8SG ideal for transceiver line cards in current and next generation multi-carrier 3G base stations.

Pin Configuration

Pin No.	Label
1	Vref
3	Input
6, 7	Output
8	Vbias
Backside Paddle	GND
2, 4, 5	N/C or GND

Not Recommended for New Designs

Recommended Replacement Part: TQP7M9104

Ordering Information

Part No.	Description
AH312-S8G	High Linearity InGaP HBT Amplifier

Standard tape / reel size = 1000 pieces on a 7” reel

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	-65 to 150°C
RF Input Power, CW, 50Ω, T=25°C	+28 dBm
Device Voltage (V_{CC})	+8 V
Device Current	1400 mA
Device Power	8 W
Junction Temperature	+200°C

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Device Voltage (V_{CC})	4.75	5.0	5.25	V
I_{cc}		800		mA
Case Temperature	-40		+85	°C
Tj for >10^6 hours MTTF			+200	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Test conditions unless otherwise noted: V_{CC}=+5 V, Temp= +25°C, tuned application circuit

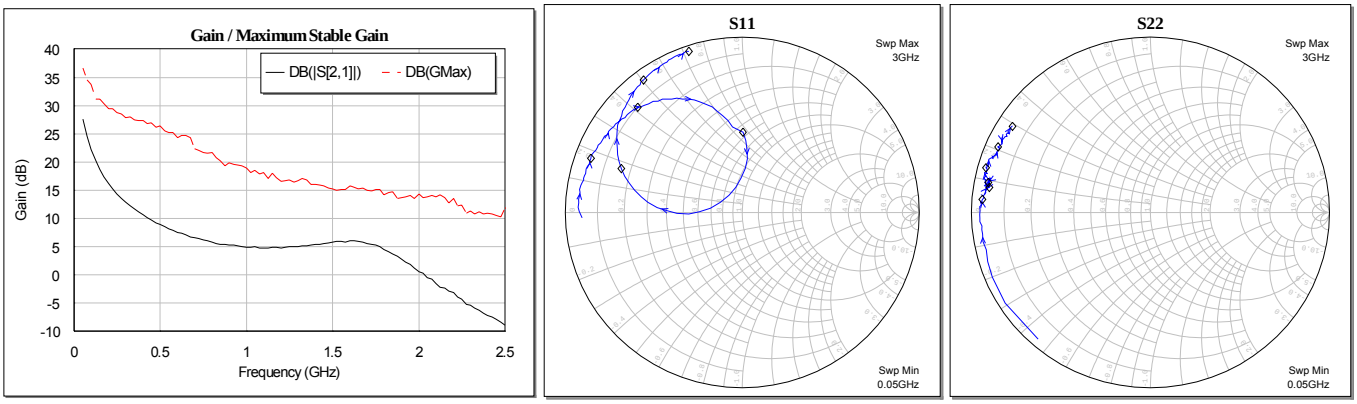
Parameter	Conditions	Min	Typ	Max	Units
Operational Frequency Range		400		2300	MHz
Test Frequency			2140		MHz
Gain		9	10		dB
Input R.L.			20		dB
Output R.L.			6.8		dB
Output P1dB		+32	+33.2		dBm
Output IP3	Pout = +17 dBm/tone, Δf=1 MHz	+47	+48		dBm
WCDMA Channel Power (1)	ACLR= -45 dBc		+25.3		dBm
Noise Figure			7.7		dB
Operating Current Range, Icc (2)		700	800	900	mA
Thermal Resistance, Θ_{JC}	Junction to backside paddle		17.5		°C

Notes:

1. ACLR Test set-up: 3GPP WCDMA, TM1+64 DPCH, +5 MHz offset, PAR = 10.2 dB at 0.01% Probability.
2. This corresponds to the quiescent current or operating current under small-signal conditions into pins 6, 7, and 8. It is expected that the current can increase by an additional 200 mA at P1dB. Pin 1 is used as a reference voltage for the internal biasing circuitry. It is expected that Pin 1 will pull 22mA of current when used with a series bias resistor of R1=15Ω. (ie. total device current typically will be 822 mA.)

Device Characterization Data

S-Parameters (V_{CC} = +5 V, I_{CC} = 800 mA, T = 25 °C, calibrated to device leads)



Notes:

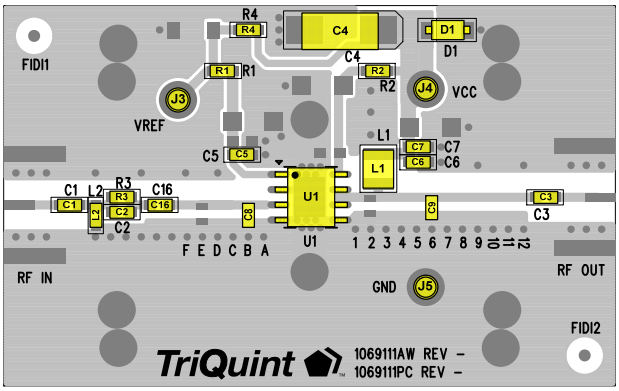
The gain for the unmatched device in 50 ohm system is shown as the trace in black color. For a tuned circuit for a particular frequency, it is expected that actual gain will be higher, up to the maximum stable gain. The maximum stable gain is shown in the dashed red line. The impedance plots are shown from 50 – 3000 MHz, with markers placed at 0.5 – 3.0 GHz in 0.5 GHz increments.

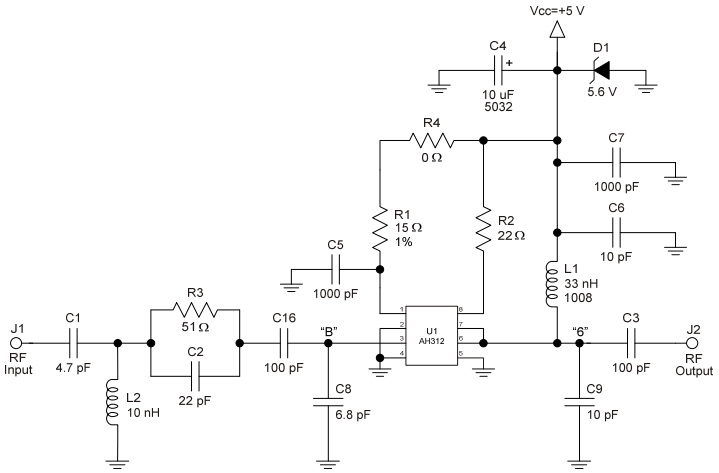
S-Parameters

Test Conditions: V_{CC} = +5 V, I_{CC} = 800 mA, T = 25 °C, unmatched 50 ohm system, calibrated to device leads)

Freq (GHz)	S11 (dB)	S11 (ang)	S21 (dB)	S21 (ang)	S12 (dB)	S12 (ang)	S22 (dB)	S22 (ang)
50	-0.86	-178.06	27.55	113.72	-45.75	30.91	-0.38	-130.98
100	-0.64	178.18	22.16	98.81	-45.46	12.80	-0.38	-157.30
200	-0.68	172.85	16.13	89.06	-42.65	6.09	-0.48	-172.51
400	-0.76	164.33	10.61	77.31	-43.96	4.69	-0.48	177.51
600	-0.93	155.56	7.46	67.94	-41.17	6.70	-0.61	173.63
800	-1.15	146.04	5.78	57.62	-41.65	-5.78	-0.66	170.49
1000	-1.50	134.58	4.87	46.90	-40.36	-7.84	-0.71	169.31
1200	-2.39	121.66	4.74	32.96	-40.22	-16.51	-0.80	168.22
1400	-4.47	104.01	5.33	14.01	-38.97	-48.82	-0.76	167.91
1600	-11.96	86.06	5.96	-17.55	-38.96	-86.32	-0.60	170.63
1800	-8.66	-179.11	4.41	-56.78	-39.35	-144.53	-0.52	167.41
2000	-2.76	159.91	0.53	-89.86	-43.55	145.94	-0.41	164.50
2200	-1.21	142.90	-3.21	-107.99	-41.56	104.25	-0.54	160.11
2400	-0.68	130.93	-7.27	-123.14	-42.46	73.64	-0.68	157.84
2600	-0.43	121.91	-10.41	-134.93	-39.71	64.28	-0.73	154.66
2800	-0.32	114.61	-13.28	-143.22	-40.99	58.20	-0.73	151.14
3000	-0.29	108.16	-15.94	-149.93	-39.65	48.40	-0.79	147.52

AH312-S8PCB900 Evaluation Board (860−940 MHz)





Notes:

1. 0 Ω jumpers may be replaced with copper traces in the target application layout.
2. On Triquint PCB 1069111, critical placement of components C8 and C9 is indicated by the alphanumeric locators on the PCB and noted on the schematic.
3. See Evaluation Board PCB Information section for PCB 1069111 material and stack-up.
4. Electrical lengths for critical component placement:
   Distance from C8 centerline to U1 pin 3: 3.66° at 900 MHz
   Distance from C9 centerline to U1 pins 6,7: 13.43° at 900 MHz

Bill of Material − AH312-S8PCB900

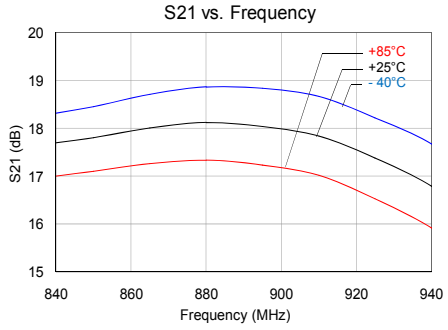
Ref. Des.	Value	Description	Manufacturer	Part Number
U1	n/a	High Linearity Amplifier	TriQuint	AH312-S8G
C1	4.7 pF	Cap, Chip, 0603, 50V, ± 0.1 pF, NPO/COG	various	
C2	22 pF	Cap, Chip, 0603, 50V, 5%, NPO/COG	various	
C3, C16	100 pF	Cap, Chip, 0603, 50V, 5%, NPO/COG	various	
C4	10 uF	Cap, Chip, 6032, 25V, 20%, TANT	various	
C5, C7	1000 pF	Cap, Chip, 0603, 50V, 5%, X7R	various	
C6	10 pF	Cap, Chip, 0603, 50V, 5%, NPO/COG	various	
C8	6.8 pF	Cap, Chip, 0603, 50V, ± 0.1 pF, Accu-P	AVX	06035J6R8BBSTR
C9	10 pF	Cap, Chip, 0603, 50V, 2%, ACCU-P	AVX	06035J100GBSTR
L1	33 nH	Coil, Wire Wound, 1008, RoHS, 5%	Coilcraft	1008HQ-33NXJLC
L2	10 nH	Ind, Chip, 0603, 5%, Cer Core	various	
R1	15 Ω	Res, Chip, 0603, 5%, 1/16W	various	
R2	22 Ω	Res, Chip, 0603, 5%, 1/16W	various	
R3	51 Ω	Res, Chip, 0603, 5%, 1/16W	various	
R4	0 Ω	Res, Chip, 0603, 5%, 1/16W	various	
D1	5.6 V	Zener Diode, SOD123, Series	On Semiconductor	MMSZ5232BT1G

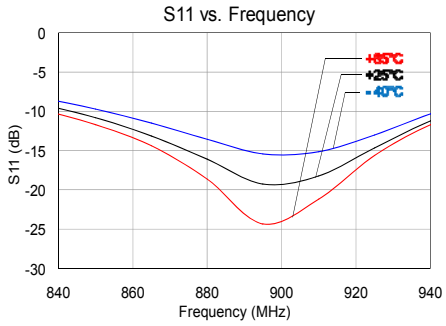
Typical Performance – AH312-S8PCB900

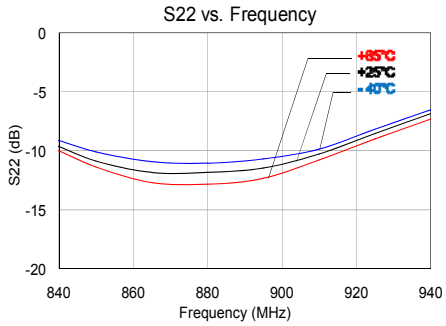
Test conditions unless otherwise noted: V_{CC} = +5 V, I_{CQ} = 800 mA, T_{LEAD} = 25°C

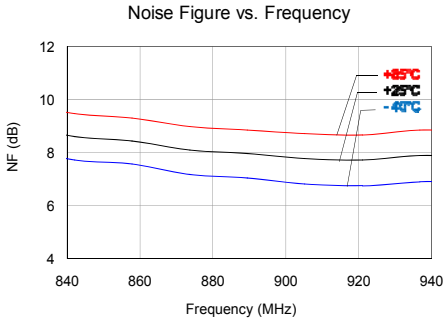
Parameter	Conditions	Typical Value			Units
Frequency		860	900	940	MHz
Gain		18	18	16.8	dB
Input Return Loss		12.5	18	12	dB
Output Return Loss		12	11	8	dB
Noise Figure		8.4	7.9	8	dB
Output P1dB		+33.5	+33	+32	dBm
Channel Power	at -45 dBc ACPR	+27	+27	+27	dBm
OIP3	Pout= +17 dBm/Tone, Δf = 1 MHz	+47	+47	+45	dBm

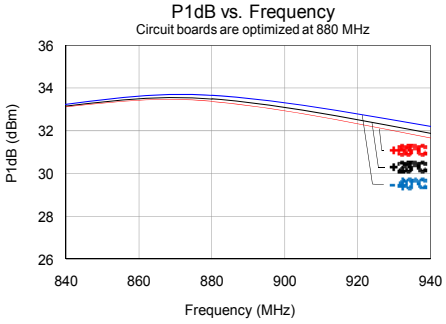
Performance Plots – AH312-S8PCB900

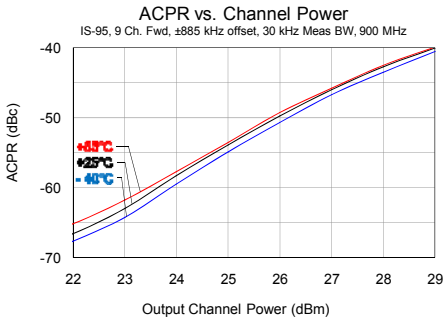


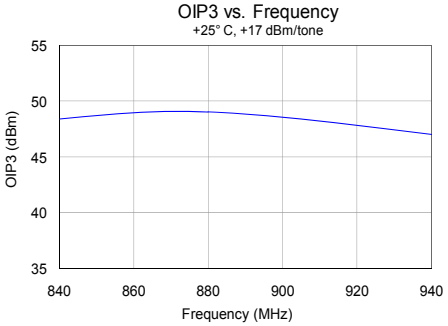


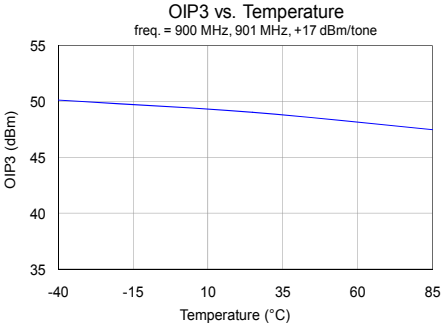


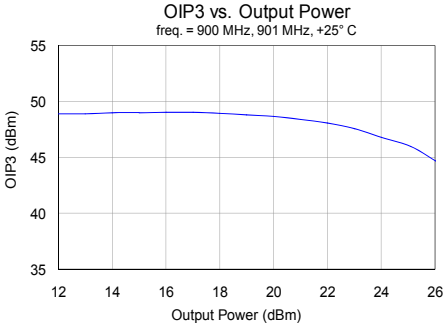




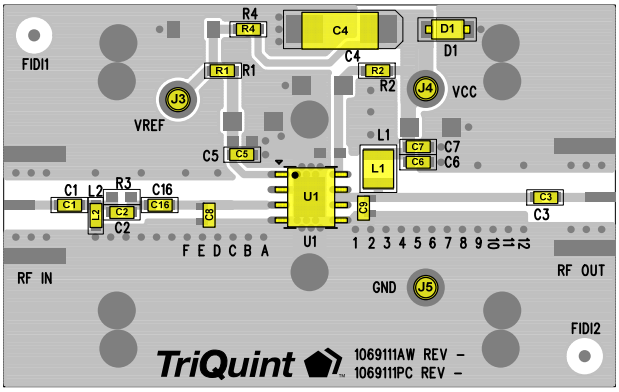


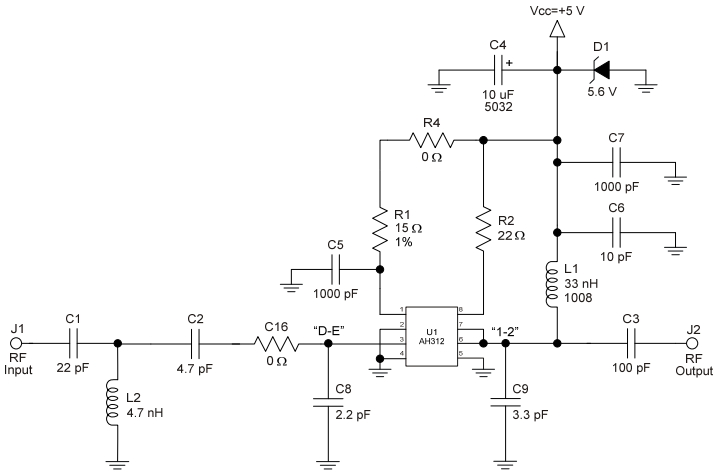






AH312-S8PCB1960 Evaluation Board (1930−1990 MHz)





Notes:

1. 0 Ω jumpers may be replaced with copper traces in the target application layout.
2. On Triquint PCB 1069111, critical placement of components C8 and C9 is indicated by the alphanumeric locators on the PCB and noted on the schematic.
3. See Evaluation Board PCB Information section for PCB 1069111 material and stack-up.
4. Electrical lengths for critical component placement:
   Distance from C8 centerline to U1 pin 3: 21.4° at 1960 MHz
   Distance from C9 centerline to U1 pins 6,7: 5.4° at 1960 MHz

Bill of Material − AH312-S8PCB1960

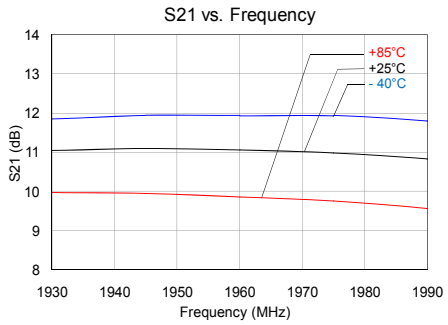
Ref. Des.	Value	Description	Manufacturer	Part Number
U1	n/a	High Linearity Amplifier	TriQuint	AH312-S8G
C1	22 pF	Cap, Chip, 0603, 50V, 5%, NPO/COG	various	
C2	4.7 pF	Cap, Chip, 0603, 50V, ± 0.1 pF, NPO/COG	various	
C3	100 pF	Cap, Chip, 0603, 50V, 5%, NPO/COG	various	
C4	10 uF	Cap, Chip, 6032, 25V, 20%, TANT	CAL-CHIP	TCMIE106CT-LF
C5, C7	1000 pF	Cap, Chip, 0603, 50V, 5%, X7R	various	
C6	10 pF	Cap, Chip, 0603, 50V, 5%, NPO/COG	various	
C8	2.2 pF	Cap, Chip, 0603, 50V, ± 0.05 pF Accu-P	AVX	06035J2R2ABSTR
C9	3.3 pF	Cap, Chip, 0603, 50V, ± 0.05 pF Accu-P	AVX	06035J3R3ABSTR
C16	0 Ω	Res, Chip, 0603, 5%, 1/16W	various	
L1	18 nH	Coil, Wire Wound, 1008, RoHS, 5%	Coilcraft	1008HQ-18NXJLC
L2	4.7 nH	Coil, Wire Wound, 0603, RoHS, 5%	Coilcraft	0603CS-4N7XJLC
R1	15 Ω	Res, Chip, 0603, 5%, 1/16W	various	
R2	22 Ω	Res, Chip, 0603, 5%, 1/16W	various	
D1	5.6 V	Zener Diode, SOD123, Series	On Semiconductor	MMSZ5232BT1 G

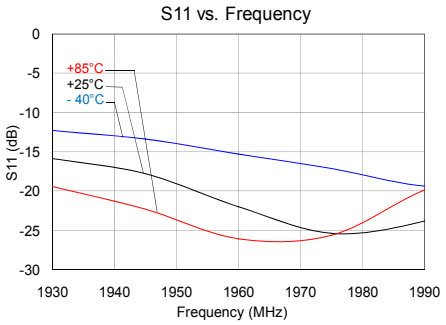
Typical Performance – AH312-S8PCB1960

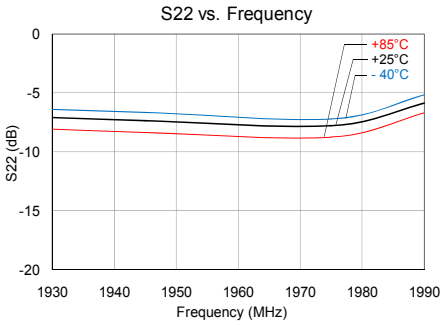
Test conditions unless otherwise noted: V_{CC} = +5 V, I_{CQ} = 800 mA, T_{LEAD} = 25 °C

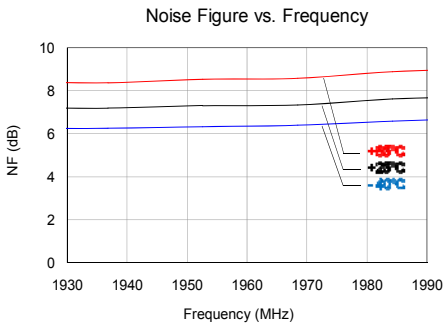
Parameter	Conditions	Typical Value			Units
Frequency		1930	1960	1990	MHz
Gain		11	11	10.9	dB
Input Return Loss		16	22	24	dB
Output Return Loss		7.5	7.6	6	dB
Noise Figure		7	7.3	7.5	dB
Output P1dB		+33	+33.4	+33	dBm
Channel Power	at -45 dBc ACPR	+27.5	+27.5	+27.5	dBm
OIP3	Pout= +17 dBm/Tone, Δf = 1 MHz	+52	+54	+53	dBm

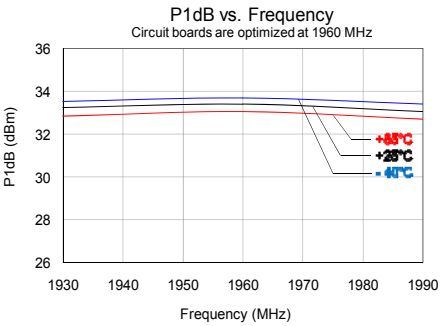
Performance Plots – AH312-S8PCB1960

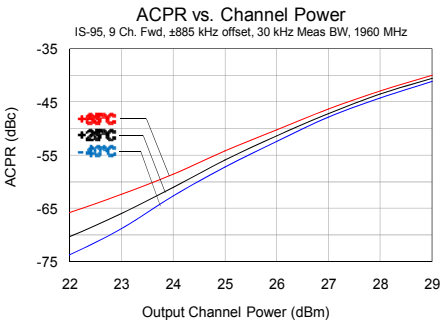


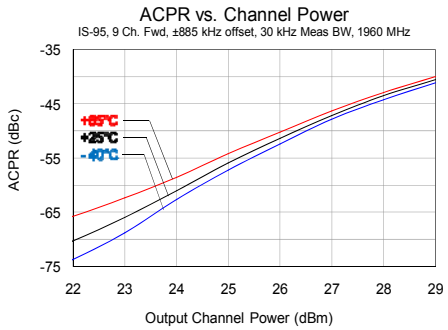


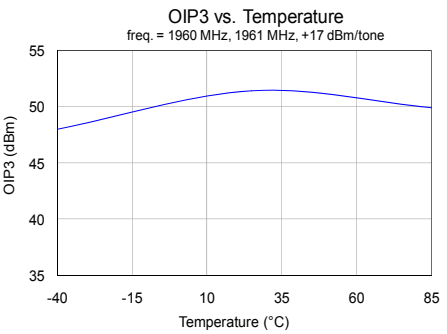


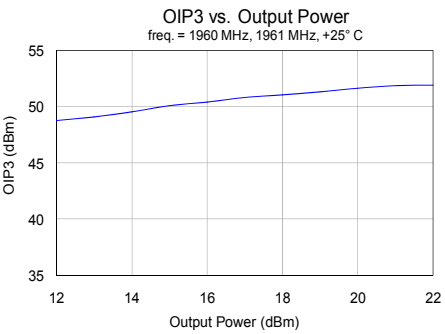




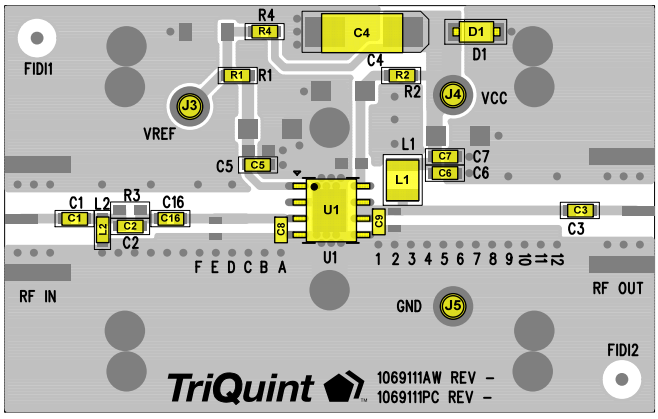


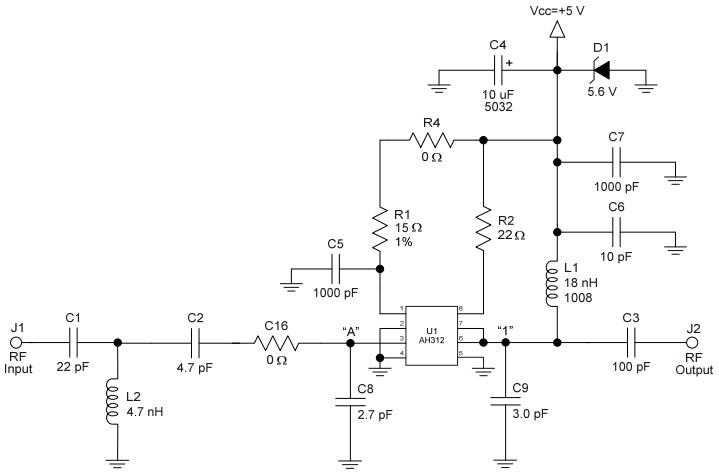






Evaluation Board – AH312-S8PCB2140





Notes:

1. 0 Ω jumpers may be replaced with copper traces in the target application layout.
2. On Triquint PCB 1069111, critical placement of components C8 and C9 is indicated by the alphanumeric locators on the PCB and noted on the schematic.
3. See Evaluation Board PCB Information section for PCB 1069111 material and stack-up.
4. Electrical lengths for critical component placement:.
   Distance from C8 centerline to U1 pin 3: 2.9° at 2140 MHz
   Distance from C9 centerline to U1 pins 6,7: 2.9° at 2140 MHz

Bill of Material – AH312-S8PCB2140

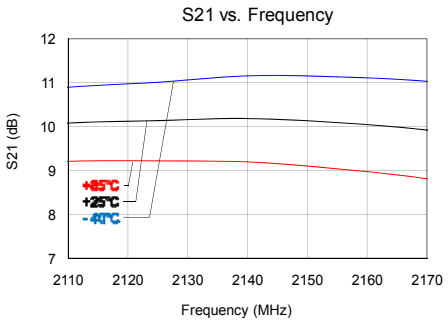
Ref. Des.	Value	Description	Manufacturer	Part Number
U1	n/a	High Linearity Amplifier	TriQuint	AH312-S8G
C1	22 pF	Cap, Chip, 0603, 50V, 5%, NPO/COG	various	
C2	4.7 pF	Cap, Chip, 0603, 50V, ± 0.1 pF, NPO/COG	various	
C3	100 pF	Cap, Chip, 0603, 50V, 5%, NPO/COG	various	
C4	10 uF	Cap, Chip, 6032, 25V, 20%, TANT	CAL-CHIP	TCMIE106CT-LF
C5, C7	1000 pF	Cap, Chip, 0603, 50V, 5%, X7R	various	
C6	10 pF	Cap, Chip, 0603, 50V, 5%, NPO/COG	various	
C8	2.7 pF	Cap, Chip, 0603, 50V ± 0.05 pF Accu-P	AVX	06035J2R7ABSTR
C9	3.0 pF	Cap, Chip, 0603, 50V ± 0.05 pF Accu-P	AVX	06035J3R0ABSTR
C16, R4	0 Ω	Res, Chip, 0603, 5%, 1/16W	various	
L1	18 nH	Coil, Wire Wound, 1008, RoHS, 5%	Coilcraft	1008HQ-18NXJLC
L2	4.7 nH	Coil, Wire Wound, 0603, RoHS, 5%	Coilcraft	0603CS-4N7XJLC
R1	15 Ω	Res, Chip, 0603, 5%, 1/16W	various	
R2	22 Ω	Res, Chip, 0603, 5%, 1/16W	various	
D1	5.6 V	Zener Diode, SOD123, Series	On Semiconductor	MMSZ5232BT1G

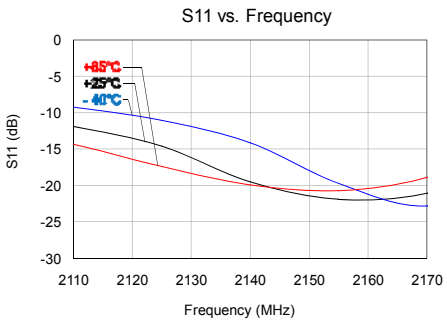
Typical Performance – AH312-S8PCB2140

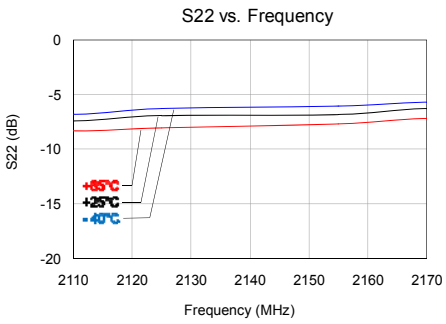
Test conditions unless otherwise noted: V_{CC} = +5 V, I_{CQ} = 800 mA, T_{LEAD} = 25°C

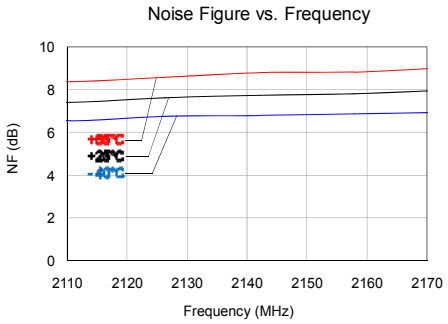
Parameter	Conditions	Typical Value			Units
Frequency		2110	2140	2170	MHz
Gain		10.1	10.2	10	dB
Input Return Loss		12	20	22	dB
Output Return Loss		7	7	7	dB
Noise Figure		7.7	7.9	8	dB
Output P1dB		+33.1	+33	+32.9	dBm
Channel Power	at -45 dBc ACPR	+25.3	+25.3	+25.3	dBm
OIP3	Pout +17 dBm/Tone, Δf = 1 MHz	+48	+48	+48	dBm

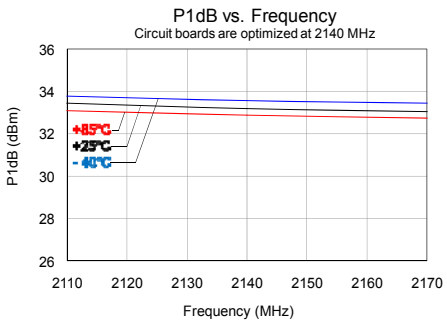
Performance Plots – AH312-S8PCB2140

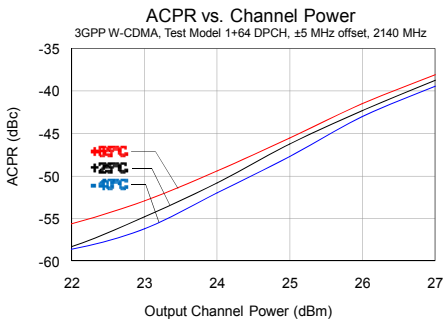


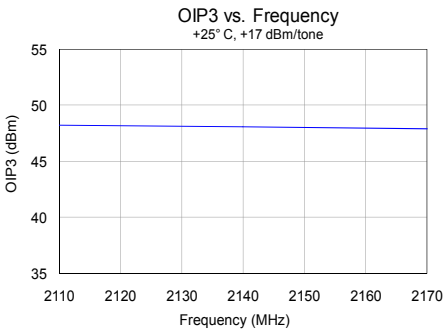


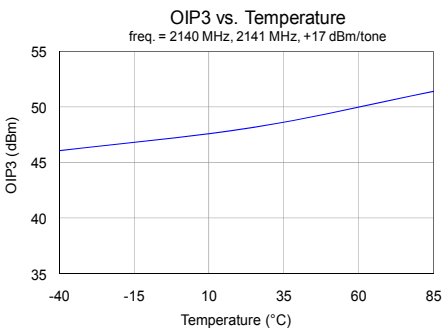


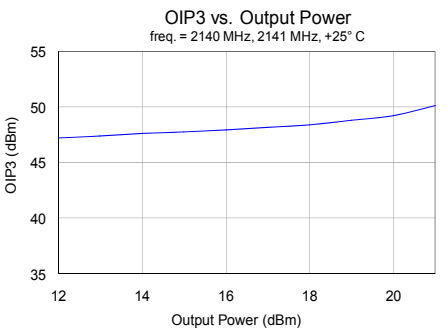








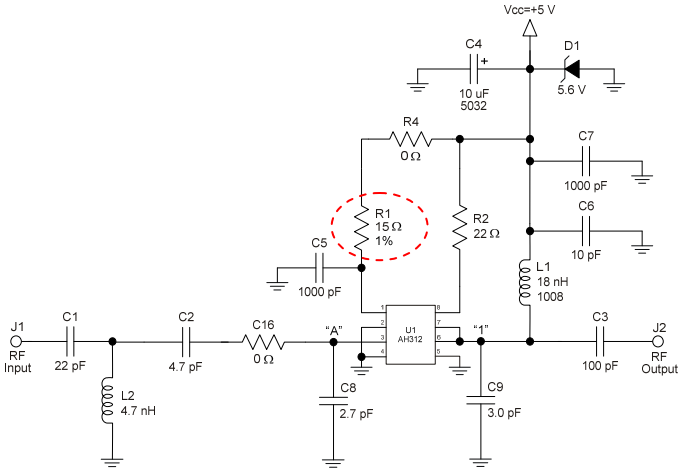




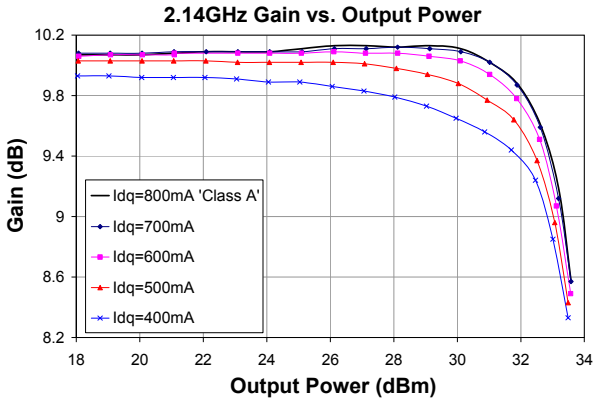
Application Note – Reduced Bias Configurations AH312-S8PCB2140

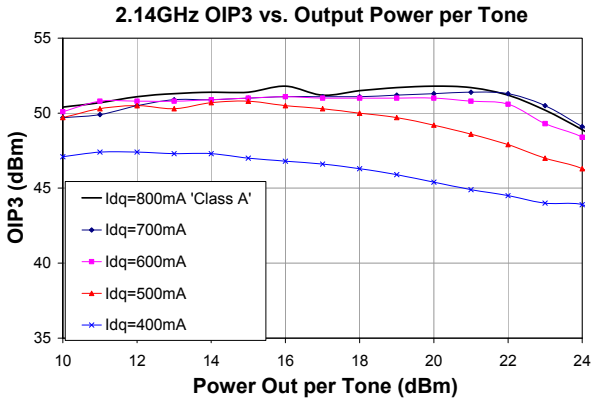
The AH312 can be configured to be operated with lower bias current by varying the bias-adjust resistor – R1. The recommended circuit configurations shown previously in this datasheet have the device operating in Class A operation. Lowering the current has little effect on the gain, OIP3, and P1dB performance of the device, but will slightly lower the ACLR/ACPR performance of the device as shown below. An example of the measured data below represents the AH312 measured and configured for 2.14 GHz applications. It is expected that variation of the bias current for other frequency applications will produce similar performance results.

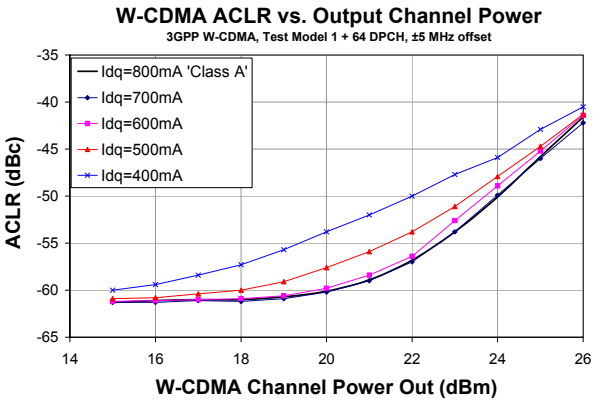
R1 (Ohms)	Icq (mA)	Pdiss (W)	P1dB (dBm)	OIP3 (dBm)
15	800	4.0	+33.3	+51.4
22	700	3.5	+33.3	+50.9
43	600	3.0	+33.1	+50.9
62	500	2.5	+33.0	+50.7
110	400	2.0	+32.9	+47.3

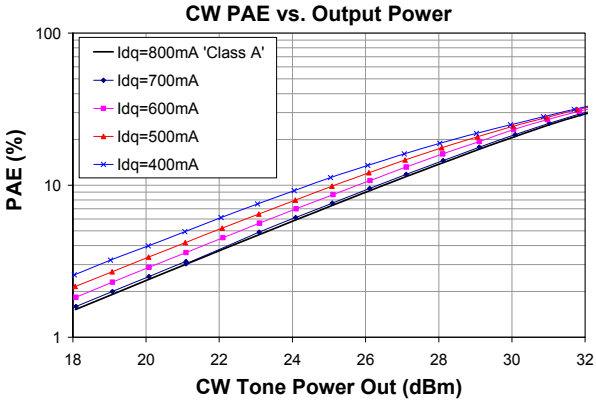


Performance Plots – AH312-S8PCB2140

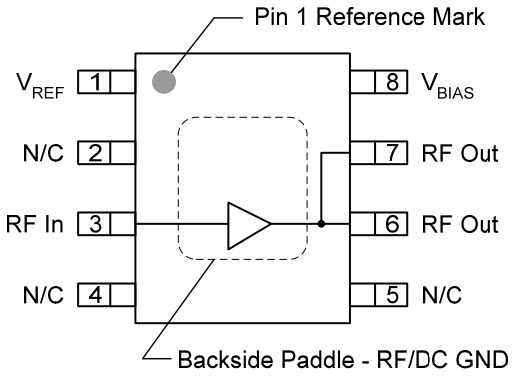








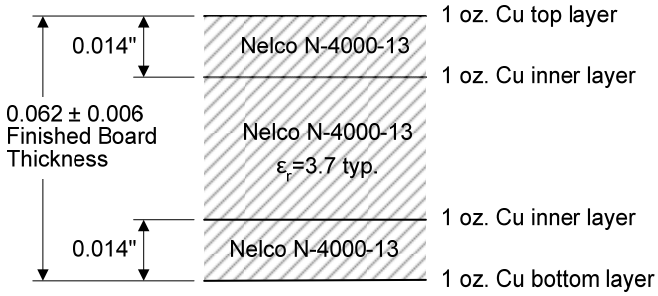
Pin Configuration and Description



Pin No.	Label	Description
1	Vref	Set reference current
2, 4, 5	N/C or GND	No electrical connection. Provide a grounded solder pad for mounting
3	RF Input	RF Input. Requires matching circuit to 50 Ω. See application circuits.
6, 7	RF Output	RF Output. Requires matching circuit to 50 Ω. See application circuits.
8	Vbias	Sets operating current.
Backside Paddle	RF/DC GND	Backside Paddle. Multiple vias should be employed to minimize inductance and thermal resistance. See PCB Mounting Pattern for suggested footprint.

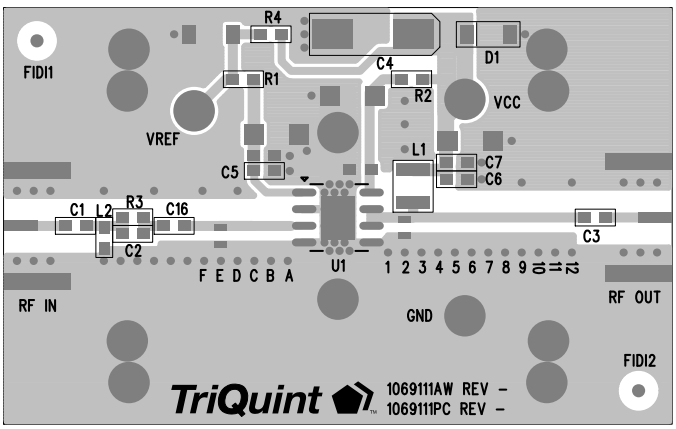
Evaluation Board PCB Information

TriQuint PCB 1095178 Material and Stack-up



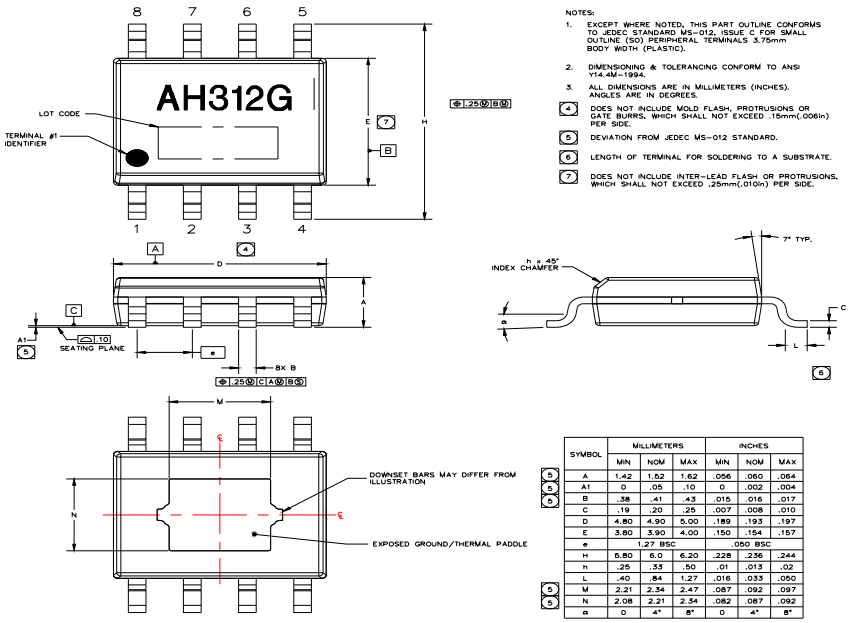
Microstrip line details: width = .026”, spacing = .026”

The silk screen markers ‘A’, ‘B’, ‘C’, etc. and ‘1’, ‘2’, ‘3’, etc. are used as place markers for critical tuning components. The markers and vias are spaced in .050” increments.



Package Marking and Dimensions

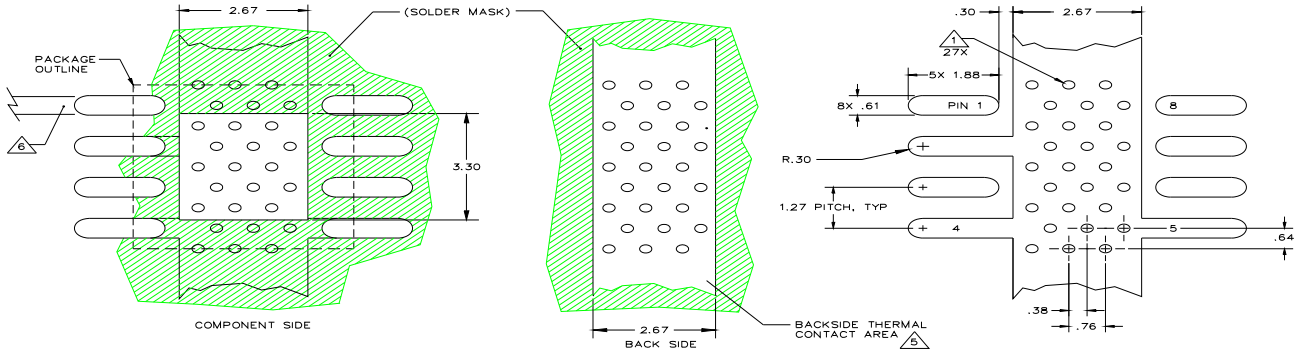
The component will be marked with an "AH312G" designator with an alphanumeric lot code on the top surface of the package.



NOTES:
1. EXCEPT WHERE NOTED, THIS PART OUTLINE CONFORMS TO JEDEC STANDARD MS-012, ISSUE C FOR SMALL OUTLINE (SO) PERIPHERAL TERMINALS 3.75mm BODY WIDTH (PLASTIC).
2. DIMENSIONING & TOLERANCING CONFORM TO ANSI Y14.5M-1994.
3. ALL DIMENSIONS ARE IN MILLIMETERS (INCHES). ANGLES ARE IN DEGREES.
4. DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS, WHICH SHALL NOT EXCEED .15mm(.006in) PER SIDE.
5. DEVIATION FROM JEDEC MS-012 STANDARD.
6. LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
7. DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS, WHICH SHALL NOT EXCEED .25mm(.010in) PER SIDE.

SYMBOL	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.42	1.52	1.62	.056	.060	.064
A1	0	.05	.10	0	.002	.004
B	.38	.41	.43	.015	.016	.017
C	.19	.20	.25	.007	.008	.010
D	4.80	4.90	5.00	.189	.193	.197
E	3.80	3.90	4.00	.150	.154	.157
e	1.27 BSC			.050 BSC		
H	5.80	6.0	6.20	.228	.236	.244
h	.25	.33	.50	.01	.013	.02
L	.40	.84	1.27	.016	.033	.050
M	2.21	2.34	2.47	.087	.092	.097
N	2.08	2.21	2.34	.082	.087	.092
α	0	4°	8°	0	4°	8°

PCB Mounting Pattern



Notes:

1. A heatsink underneath the area of the PCB for the mounted device is strictly required for proper thermal operation. Damage to the device can occur without the use of one.
2. Ground/thermal vias are critical for the proper performance of this device. Vias should use a .35mm (#80 / .0135") diameter drill and have a final plated thru diameter of .25 mm (.010").
3. Use 1 oz. Copper minimum. Add as much copper as possible to inner and outer layers near the part to ensure optimal thermal performance.
4. Mounting screws can be added near the part to fasten the board to a heatsink. Ensure that the ground / thermal via region contacts the heatsink.
5. Do not put solder mask on the backside of the PC board in the region where the board contacts the heatsink.
6. RF trace width depends upon the PC board material and construction.
7. All dimensions are in millimeters (inches). Angles are in degrees.
8. The pad pattern shown has been developed and tested for optimized assembly at TriQuint. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from company to company, careful process development is recommended.

Product Compliance Information

ESD Sensitivity Ratings

Caution! ESD-Sensitive Device

ESD Rating: Class 1B
Value: ≥ 500 V and <1000 V
Test: Human Body Model (HBM)
Standard: JEDEC Standard JESD22-A114

ESD Rating: Class IV
Value: Passes between greater than 1000 V
Test: Charged Device Model (CDM)
Standard: JEDEC Standard JESD22-C101-C

MSL Rating

MSL Rating: Level 3
Test: 260°C convection reflow
Standard: JEDEC Standard J-STD-020

Solderability

Compatible with both lead-free (260°C max. reflow temperature) and tin/lead (245°C max. reflow temperature) soldering processes.

Package contact plating: NiPdAu

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

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