7-16GHz High Power Amplifier

Preliminary

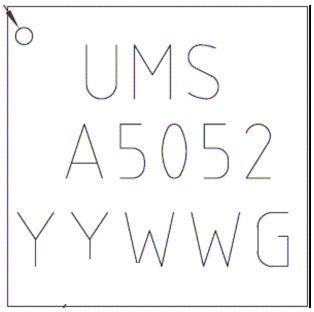
GaAs Monolithic Microwave IC in SMD package

Description

The CHA5052-QGG is a three-stage monolithic high power amplifier.

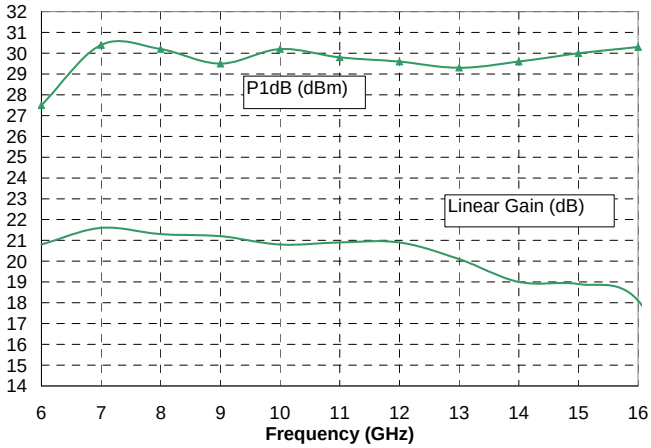
The circuit is manufactured with a power P-HEMT process, 0.15µm gate length, via holes through the substrate.

It is supppplied in RoHS compliant SMD package.



Main Features

- Frequency range 7-16GHz
- Gain: 19dB
- 37dBm 3rd order intercept point
- 29dBm Output Power @1dB compression
- ESD protected (see page 7)
- DC power consumption, 700mA @ 5V
- 28LQFN5x5



Typical on board measurements

Main Characteristics

Tamb. = 25°C, Vd = 5V

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range	7		16	GHz
G_lin	Small signal gain		19		dB
P1dB	Output power at 1dB gain compression		29		dBm
OIP3	Output IP3		37		dBm

ESD Protection: Electrostatic discharge sensitive device. Observe handling precautions!

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Electrical Characteristics

Preliminary

Tamb=25℃, Vd = 5V and Id = 700mA, CW biasing mode.
These values are representative of onboard measurements as defined on the drawing 96402

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range	7		16	GHz
G_lin	Small signal gain from 7 to 12GHz		20		dB
	from 12.5 to 16GHz		18		dB
P1dB	Output power at 1dB compression		29		dBm
Psat	Saturated output power		30		dBm
IS11I	Input return loss		1.4:1		
IS22I	Output return loss		2.0:1		
OIP3	Output IP3 from 7 to 8GHz		38		dBm
	from 9 to 16GHz		36		dBm
Vg	Negative gate bias voltage		-1.7		V
Vd 1,2,3	Positive drain bias voltage		5		V
Id	Power supply quiescent current (1)		700		mA

(1) This value is fixed by gate voltage Vg

Absolute Maximum Ratings

Tamb. = 25℃ (1)

Symbol	Parameter	Values	Unit
Vd	Maximum Drain bias voltage	+5.5	V
Id	Power supply quiescent current	800	mA
Vg	Gate bias voltage	-4 to +0.8	V
Pin	Maximum input power overdrive	+13.0	dBm
Tj	Maximum channel temperature (2)	+175	℃
Top	Operating temperature range	-40 to +80	℃
Tstg	Storage temperature range	-55 to +125	℃

(1) Operation of this device above anyone of these parameters may cause permanent damage.
(2) Thermal Resistance channel to ground paddle =26.9℃/W for Tpaddle. = +80℃

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Typical Package Sij parameters

Tamb = +25°C, Vd1=Vd2=Vd3= +4.5V, Id = 700 mA

Freq (GHz)	dB (S11)	P (S11) (°)	dB (S21)	P (S21) (°)	dB (S12)	P (S12) (°)	dB (S22)	P (S22) (°)
0,5	-1,9	152	-44,6	27	-62,4	-29	-1,7	149
1,0	-2,9	126	-48,8	-29	-84,2	-119	-1,5	118
1,5	-4,1	104	-47,8	-137	-71,5	-21	-1,5	88
2,0	-5,6	84	-35,0	78	-71,5	-112	-1,5	57
2,5	-7,1	64	-46,5	55	-71,6	111	-1,3	27
3,0	-8,5	47	-18,6	47	-83,1	-62	-1,2	-4
3,5	-9,9	29	-13,5	-17	-70,9	156	-1,2	-35
4,0	-11,4	12	-5,1	-34	-68,5	43	-1,4	-68
4,5	-12,9	-6	6,3	-95	-81,3	-119	-2,0	-104
5,0	-14,3	-24	14,0	-175	-65,3	83	-3,8	-143
5,5	-15,8	-42	18,3	103	-69,6	27	-7,9	-180
6,0	-17,5	-62	20,6	26	-69,2	94	-14,7	161
6,5	-19,8	-83	21,7	-43	-62,8	40	-18,8	-179
7,0	-22,7	-107	22,2	-107	-66,2	3	-18,0	-173
7,5	-27,2	-137	22,3	-166	-67,8	28	-17,9	177
8,0	-33,5	157	22,1	137	-62,3	-5	-18,8	164
8,5	-28,9	62	21,8	84	-67,4	-54	-20,6	149
9,0	-23,6	20	21,5	33	-69,0	-60	-23,9	141
9,5	-20,5	-9	21,3	-16	-59,5	-77	-30,3	156
10,0	-18,7	-33	21,2	-66	-62,1	-129	-28,2	-141
10,5	-18,8	-60	21,1	-115	-67,5	-153	-20,6	-146
11,0	-18,5	-83	21,0	-163	-58,0	-166	-16,9	-159
11,5	-18,1	-106	21,0	147	-59,2	162	-14,0	-175
12,0	-18,1	-125	20,9	96	-58,0	142	-12,8	168
12,5	-18,7	-143	20,6	45	-58,0	112	-12,7	148
13,0	-19,6	-158	20,2	-6	-57,9	81	-14,5	135
13,5	-20,8	-170	19,9	-60	-61,1	143	-13,5	135
14,0	-21,2	172	19,1	-114	-56,6	95	-12,1	121
14,5	-24,0	155	18,7	-167	-56,7	81	-10,7	102
15,0	-31,6	137	18,4	138	-56,1	92	-10,2	71
15,5	-40,9	-78	18,5	77	-52,6	80	-10,1	30
16,0	-24,2	-96	18,3	7	-52,7	54	-10,0	-22
16,5	-19,2	-126	16,8	-73	-51,9	50	-10,1	-86
17,0	-17,2	-148	12,8	-155	-49,1	12	-10,9	-139
17,5	-16,4	-175	7,2	130	-61,8	22	-12,5	-168
18,0	-16,7	161	0,8	60	-55,8	56	-11,4	-167
18,5	-17,8	138	-6,3	-4	-50,4	29	-6,9	174
19,0	-19,3	118	-14,4	-62	-52,2	12	-4,0	143
19,5	-21,1	92	-23,3	-111	-50,3	2	-2,6	112
20,0	-22,5	60	-33,7	-151	-49,7	1	-1,9	83
20,5	-22,7	27	-49,8	-152	-49,9	-23	-1,6	58
21,0	-21,7	-6	-49,2	-121	-54,0	-32	-1,4	35
21,5	-19,8	-34	-57,5	-144	-57,8	-4	-1,3	14
22,0	-17,9	-54	-48,3	-122	-51,6	7	-1,2	-6
22,5	-16,3	-70	-56,6	100	-50,2	-7	-1,1	-24
23,0	-15,1	-84	-54,6	86	-51,1	-19	-1,0	-41
23,5	-14,0	-95	-4,3	48	-49,5	7	-0,9	-57
24,0	-12,9	-105	-42,4	19	-46,9	-9	-0,9	-72
24,5	-11,9	-116	-39,3	-11	-45,5	-15	-87,2	-85
25,0	-11,0	-128	-41,2	-35	-43,9	-30	-79,4	-97
25,5	-10,5	-143	-44,1	-62	-44,8	-33	-76,4	-109
26,0	-11,4	-158	-40,9	-50	-42,2	-39	-79,8	-121
26,5	-14,1	-161	-41,3	-74	-41,5	-53	-75,6	-131
27,0	-14,0	-143	-47,5	-71	-42,1	-62	-73,6	-141
27,5	-11,4	-141	-42,8	-86	-41,6	-63	-69,0	-151
28,0	-9,5	-148	-42,0	-77	-39,0	-71	-65,7	-161
28,5	-8,4	-156	-38,9	-94	-37,9	-89	-65,3	-170
29,0	-7,5	-165	-36,4	-95	-37,8	-104	-77,5	-178
29,5	-6,9	-174	-3,6	-105	-37,2	-115	-90,4	173
30,0	-6,5	177	-36,7	-119	-36,6	-127	-0,9	164

Refer to the “definition of the Sij reference planes” section below

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Typical Measured Performance

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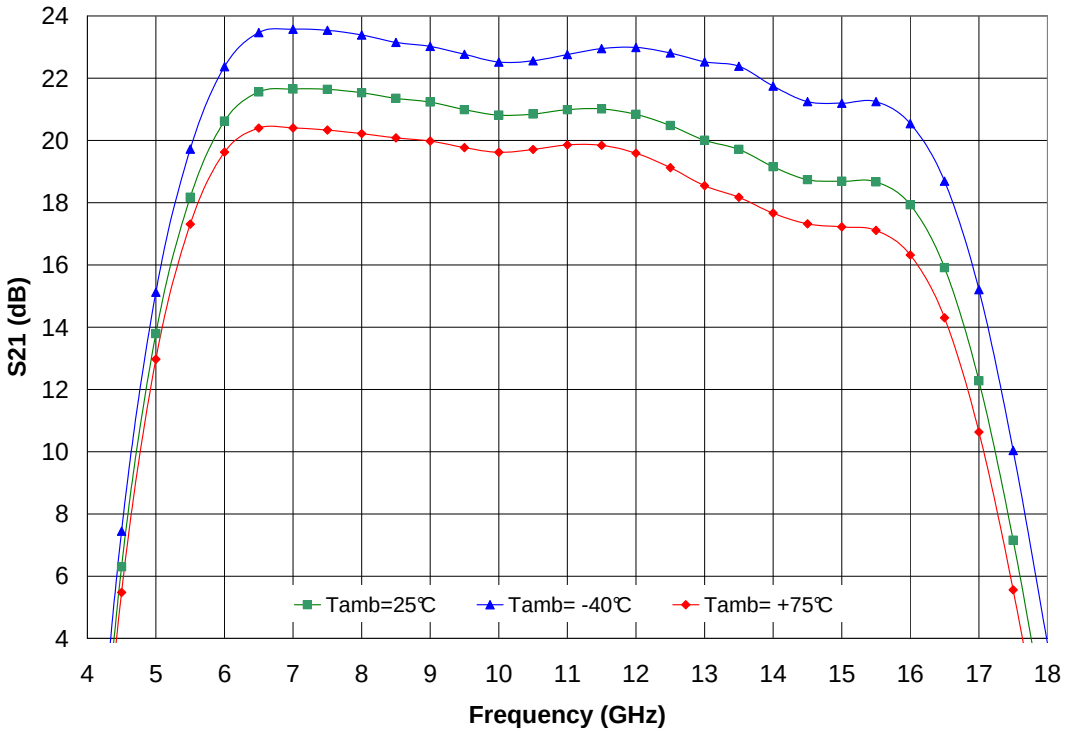
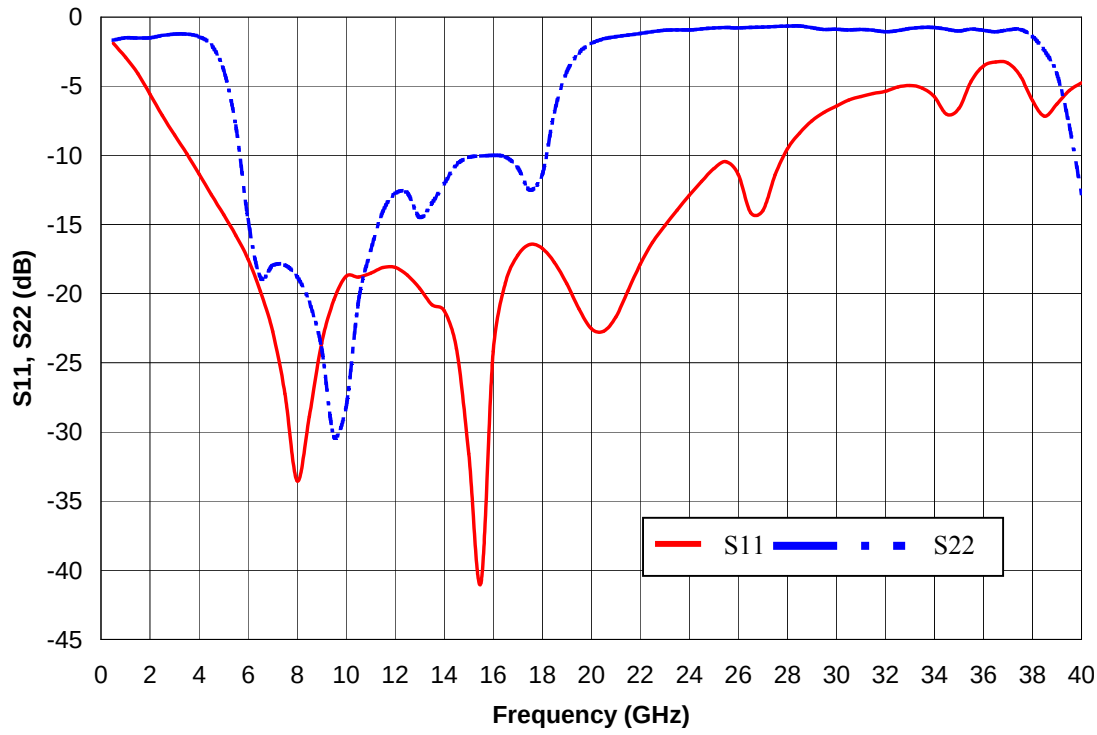
Tamb = +25℃, Vd1=Vd2=Vd3=+5V, Id (Quiescent)=700mA , CW biasing mode

Measurements in the package access planes, using the proposed land pattern & board 96402

Gain variation versus temperature



Return losses versus temperature @ 25℃



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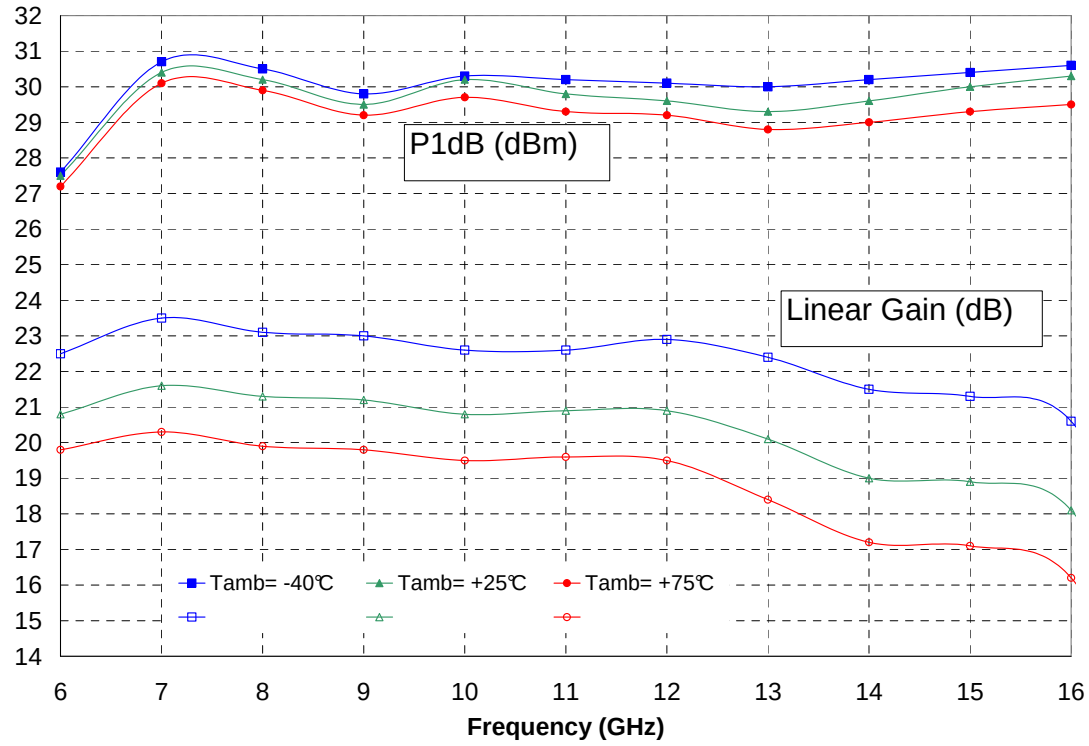
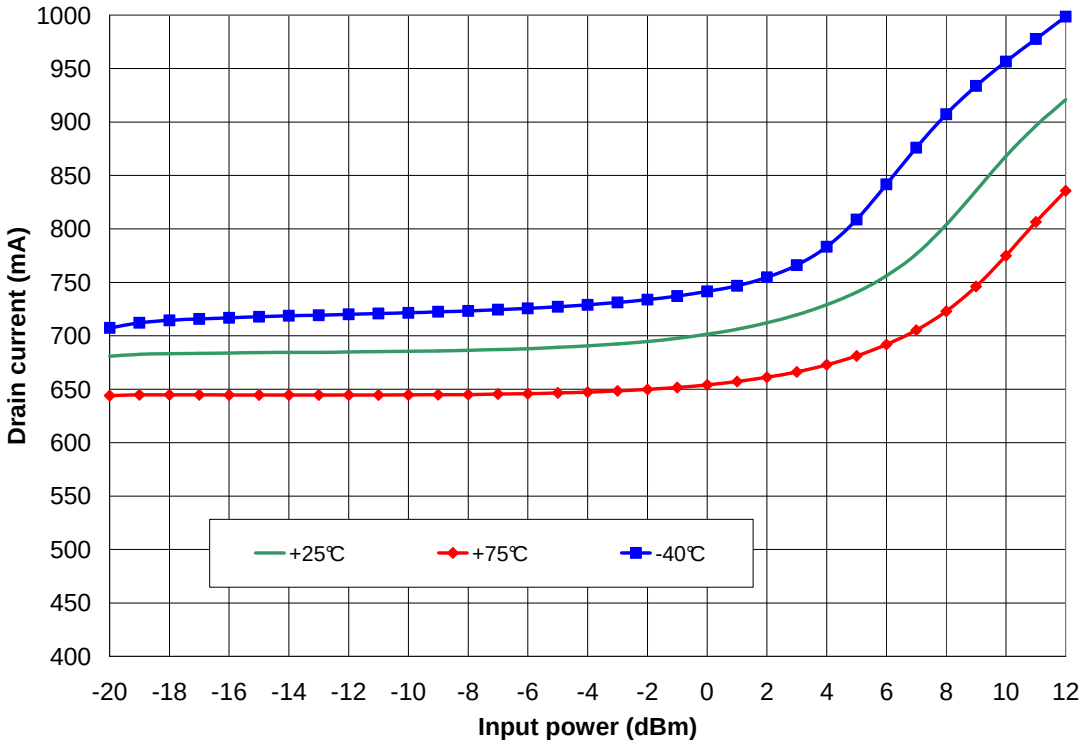
Output power@ 1dB compression & linear Gain versus temperature



Drain current versus Pin & Temperature @ RFfreq= 14GHz



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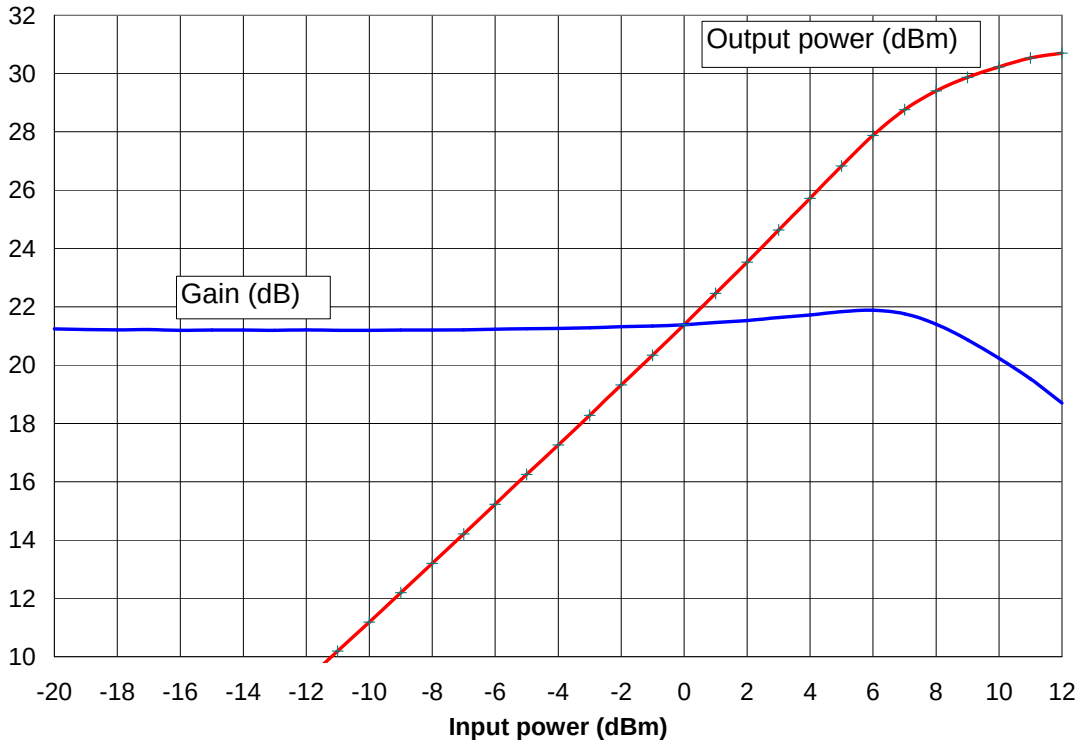
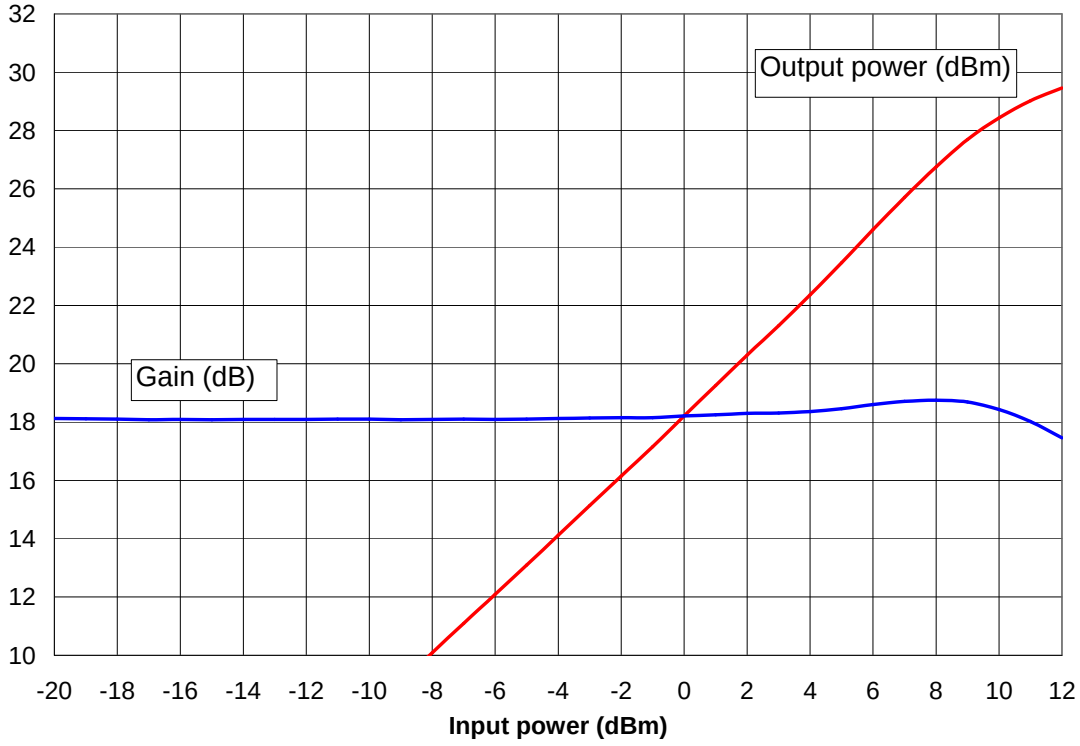
Gain & Pout versus Pin @ RFfreq=7GHz, 25°C



Gain & Pout versus Pin @ RFfreq=15GHz, 25°C



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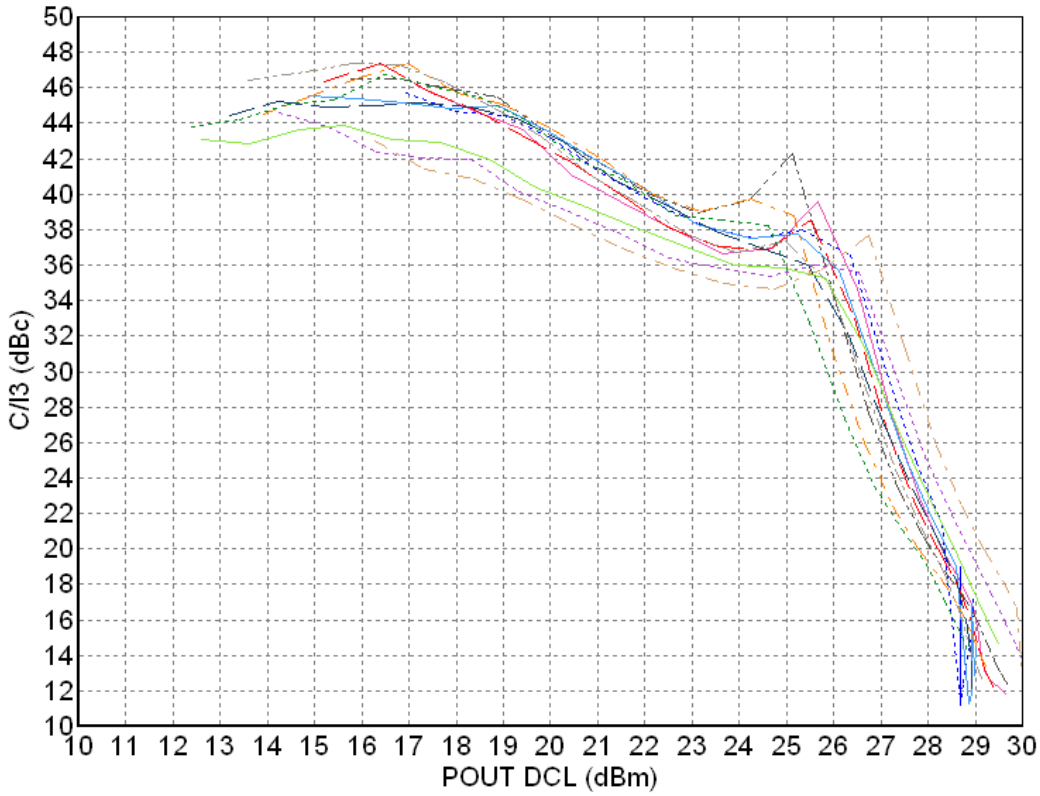
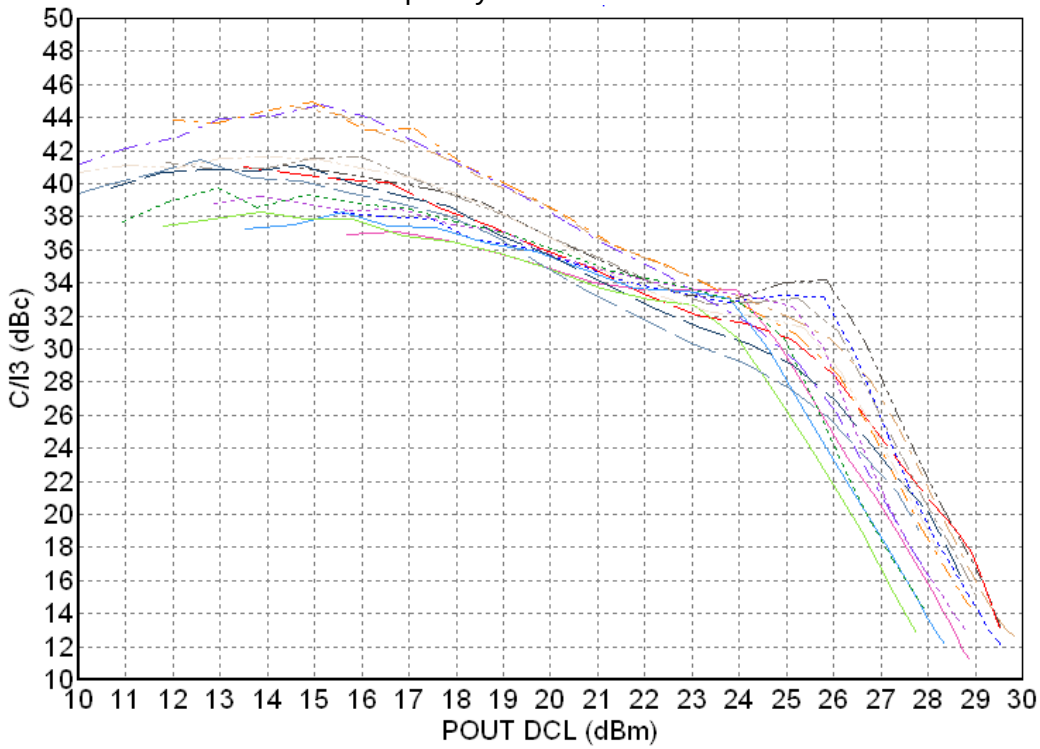
C/I3 versus Pout DCL at Temperature –40, +25, +75°C

Preliminary

Frequency 7 to 10GHz



Frequency 12 to 16GHz



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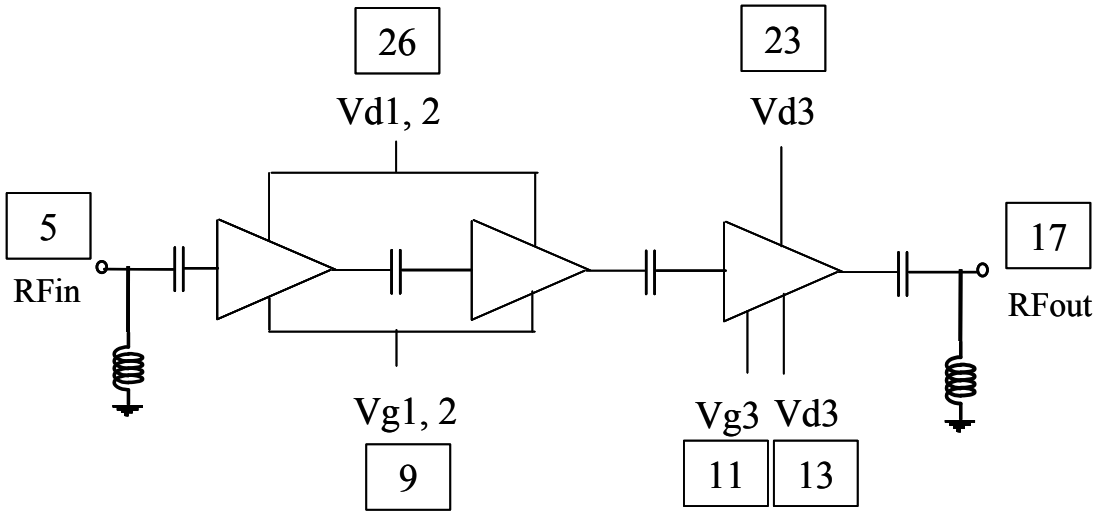
Note

Preliminary

Due to ESD protection, RFin and RFout are DC grounded, an external capacitance might be requested to isolate the product from external voltage that could be present on the RF accesses.

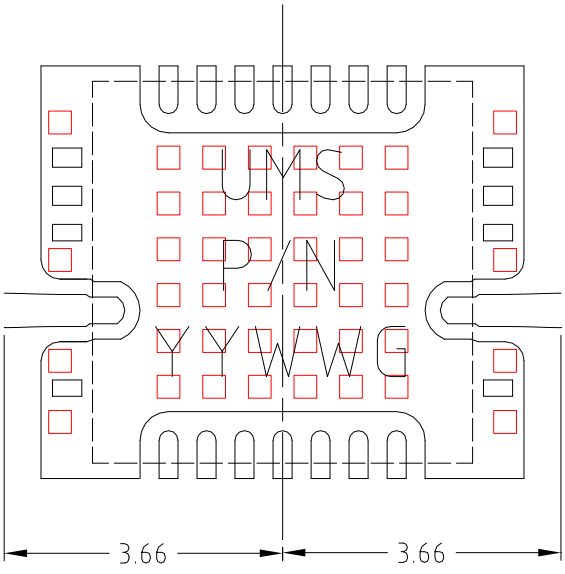


ESD protections are also implemented on gate accesses.

The DC connections do not include any decoupling capacitor in package, therefore it is mandatory to provide a good external DC decoupling on the PC board, as close as possible to the package.

Definition of the Sij reference planes

The reference planes are defined from the footprint of the recommended characterization board shown below under the number 96402.
The reference is the symmetrical axis of the package. The input and output reference planes are located at 3.66mm offset (input wise and output wise respec.) from this axis. Then, the given Sij incorporates this land pattern.



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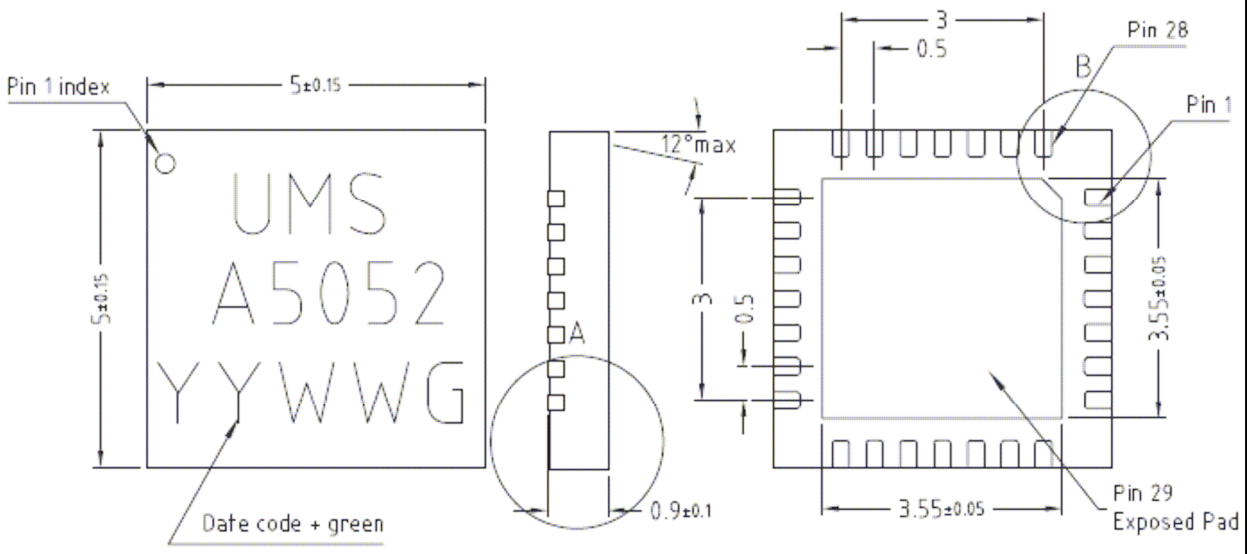
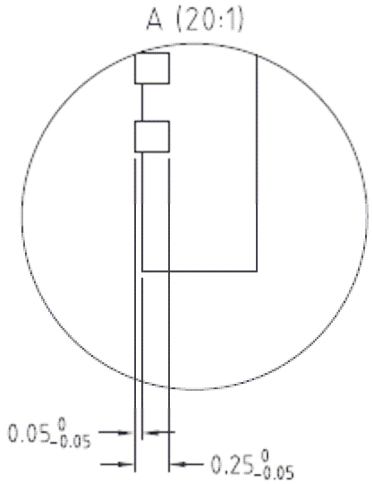
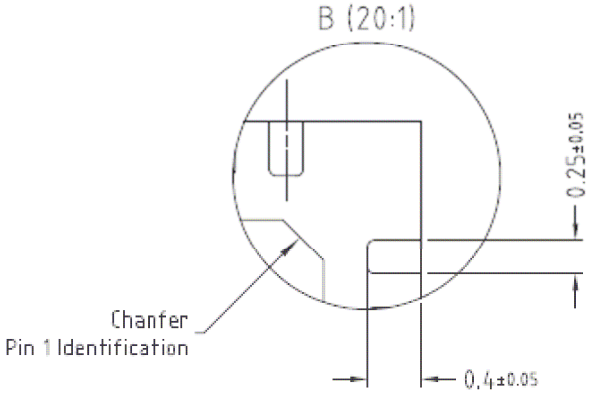
Package outline







Matt tin, Lead free (Green)
Units : mm
From the standard : JEDEC MO-220 [VEED-6]

1- Gnd	10- Nc	19- Gnd	28-Nc
2- Nc	11- VG3	20- Nc	29-GND Exposed Pad
3- Gnd	12- Nc	21- Gnd	
4- Gnd	13- VD3	22- Nc	
5- RF IN	14- Nc	23- VD3	
6- Gnd	15- Gnd	24- Nc	
7- Gnd	16- Gnd	25- Nc	
8- Nc	17- RF OUT	26- VD1-VD2	
9- VG1-VG2	18- Gnd	27- Nc	

SMD mounting procedure

The SMD leadless package has been designed for high volume surface mount PCB assembly process. The dimensions and footprint required for the PCB (motherboard) are given in the drawings above.

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017.

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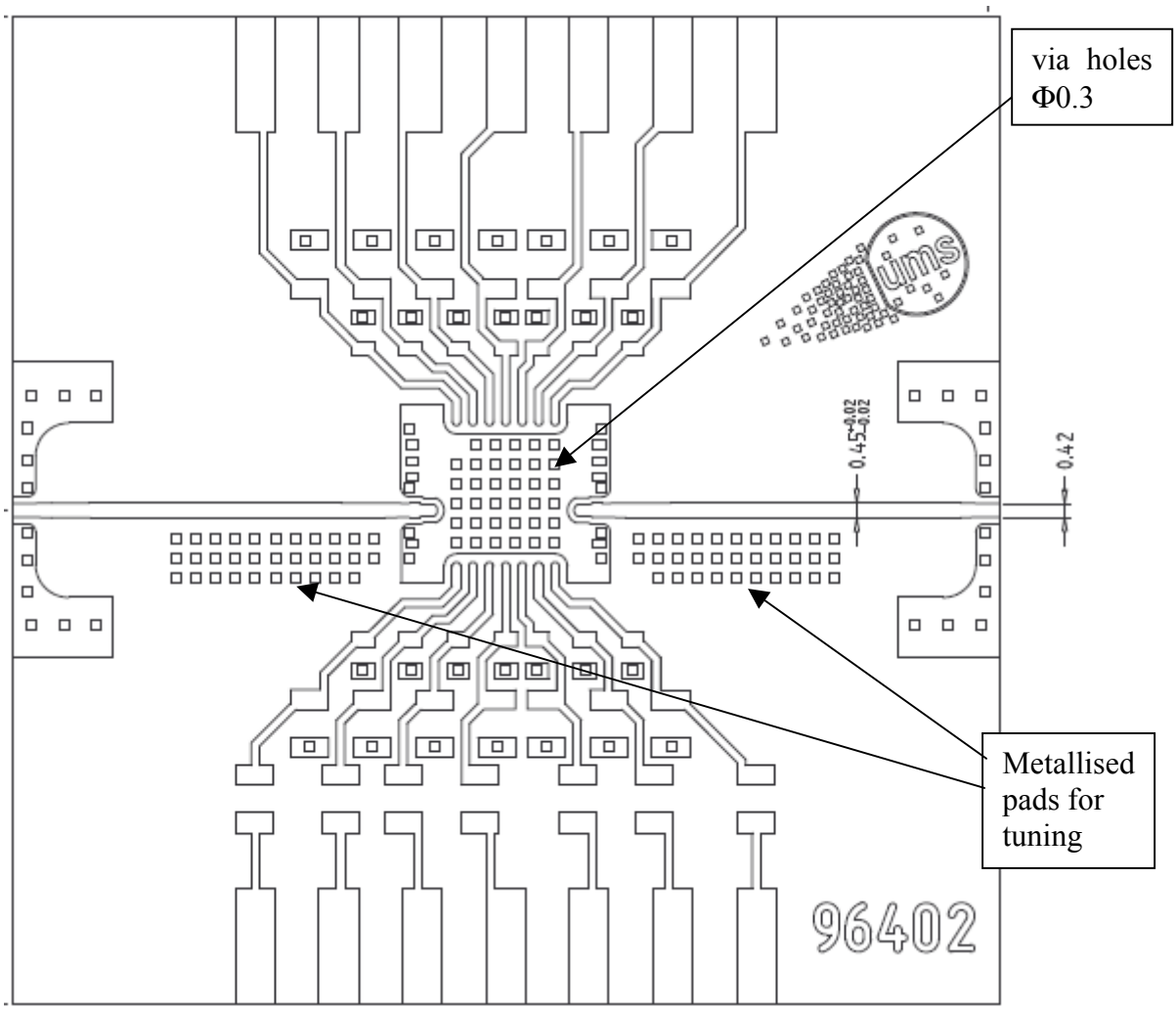
Proposed Assembly board “96402” for the 28L-QFN5x5 products characterization.

Preliminary

- Compatible with the proposed footprint.
- Based on typically Ro4003 / 8mils or equivalent.
- Using a microstrip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.



Ordering Information

QFN 5x5 RoHS compliant package: CHA5052-QGG/XY
Stick: XY = 20 Tape & reel: XY = 21

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