7-13GHz Low Noise Amplifier

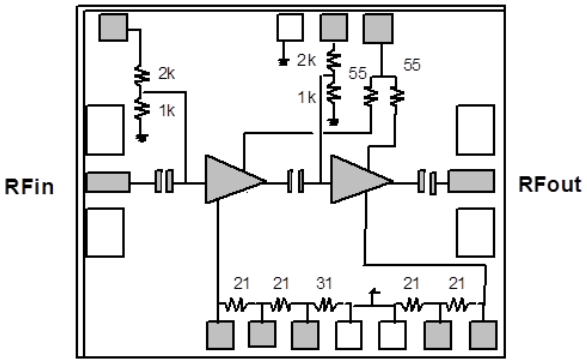
GaAs Monolithic Microwave IC

Description

The CHA2063a99F is a two-stage wide band monolithic low noise amplifier.

It is supplied in chip form The circuit is manufactured with a pHEMT process, 0.25µm gate length, via holes through the substrate, air bridges and electron beam gate lithography.

It is available in chip form.



Main Features

- Broad band performance 7-13GHz
- 2.0dB noise figure, 8-13GHz
- 19dB gain
- Low DC power consumption, 40mA
- 18dBm 3rd order intercept point
- Chip size : 1,52 x 1,27 x 0.1mm

Main Electrical Characteristics

Tamb.= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range	7		12	Ghz
G	Gain	17	19		dB
NF	Noise figure 7-8Ghz Noise figure 8-12GHz		2.5 2.0	3.0 2.5	dB

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Electrical Characteristics

Tamb.= +25°C, Vd = +4.0V

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range	7		12	Ghz
G	Gain	17	19		dB
ΔG	Gain flatness		± 2		dB
NF	Noise figure 7-8Ghz Noise figure 8-12GHz		2.5 2.0	3.0 2.5	dB
VSWRin	Input VSWR		2.0:1	3.0:1	
VSWRout	Ouput VSWR		2.0:1	3.0:1	
P1dB	Output power at 1dB gain compression @ F=10GHz		8		dBm
IP3	3rd order intercept point		18		dBm
Id	Drain bias current		40	80	mA

(1) These values are representative of on-wafer measurements that are made without bonding wires at the RF ports. When the chip is connected with typical 0.3nH input and output bonding wires, the indicated parameter values are close to those of the CHA2063a packaged product.

Absolute Maximum Ratings (1)

Tamb.= +25°C

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage (3)	5.0	V
Pin	Maximum peak input power overdrive (2)	+15	dBm
Tj	Maximum Junction temperature	175	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.
(2) Duration < 1s.
(3) See chip biasing option

Temperature Range

Ta	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +150	°C

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Typical on-wafer Sij parameters

Tamb.= +25°C
Vd = 4.0V ; Vg1 = Vg2 = +2.5V ; Id = 40mA (A,B,C,D & E not connected)
(see chip biasing option)

Freq (GHz)	S11 (dB)	PhS11 (°)	S12 (dB)	PhS12 (°)	S21 (dB)	PhS21 (°)	S22 (dB)	PhS22 (°)
5.00	-0.86	-91.7	--65.97	-63.6	6.08	-175.1	-7.99	-131.3
5.50	-1.66	-109.6	-57.28	-77.7	11.49	152.4	-9.91	-139.3
6.00	-3.56	-131.8	-50.70	-105.2	16.03	113.4	-11.62	-143.8
6.50	-7.75	-153.2	-46.25	-137.6	18.99	69.3	-12.74	-150.7
7.00	-14.77	-159.2	-43.76	-167.7	20.39	27.7	-14.62	-164.1
7.50	-21.16	-116.9	-42.21	166.7	20.79	-9.1	-18.09	-179.8
8.00	-19.40	-79.1	-41.19	145.2	20.89	-40.9	-24.49	160.0
8.50	-16.83	-61.4	-40.39	127.8	20.76	-69.6	-34.60	38.5
9.00	-14.68	-53.7	-39.78	111.7	20.45	-95.4	-23.38	-9.1
9.50	-12.52	-52.6	-39.31	96.9	20.16	-119.5	-18.53	-23.3
10.00	-10.61	-57.4	-38.85	83.9	19.79	-141.8	-15.76	-31.8
10.50	-9.31	-65.5	-38.51	72.6	19.36	-162.9	-13.58	-40.2
11.00	-8.38	-74.2	-38.14	62.0	18.85	176.6	-11.92	-48.5
11.50	-7.71	-83.7	-37.74	52.8	18.41	157.3	-10.67	-57.1
12.00	-7.26	-93.4	-37.17	44.1	17.94	138.1	-9.74	-65.8
12.50	-6.86	-103.8	-36.62	35.4	17.40	119.5	-9.01	-73.5
13.00	-6.57	-114.6	-35.91	27.3	16.84	101.6	-8.54	-81.7
13.50	-6.34	-126.4	-35.11	18.2	16.26	83.8	-8.21	-88.8
14.00	-6.18	-139.4	-34.27	8.5	15.65	66.5	-8.05	-95.7
14.50	-6.16	-153.5	-33.41	-1.9	15.01	49.1	-8.03	-101.7
15.00	-6.25	-169.0	-32.67	-13.3	14.35	31.7	-8.02	-106.9

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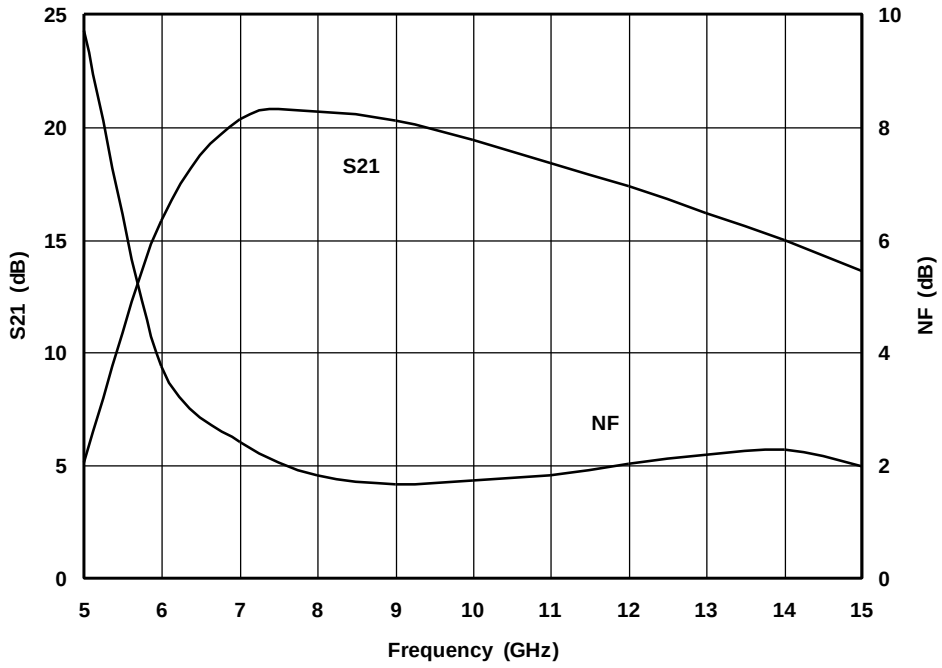
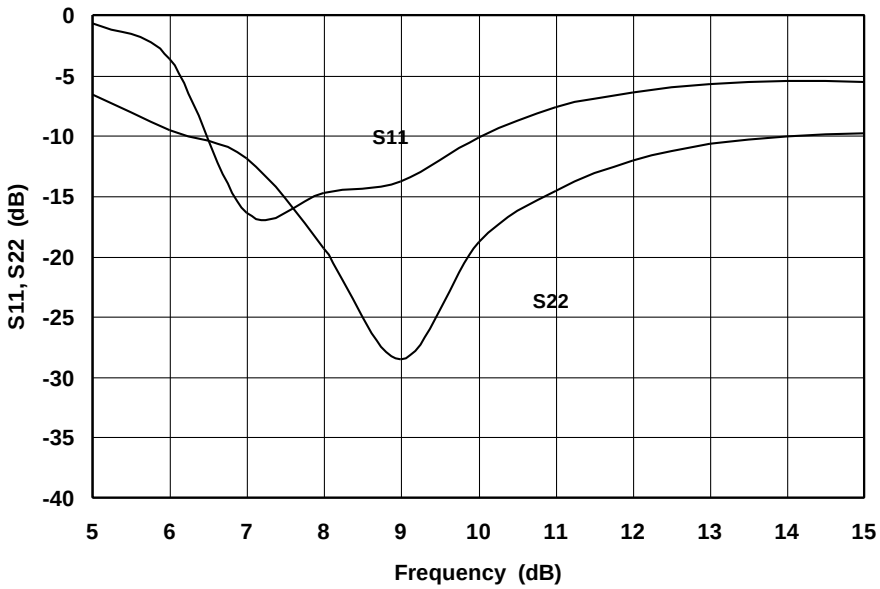
Typical on wafer Measurements

Tamb = +25°C
Vd = 4.0V ; Vg1 = Vg2 = +2.5V ; Id = 40mA (A,B,C,D & E not connected)
(see chip biasing option)

Linear Gain & Noise Figure



Input & Output matching



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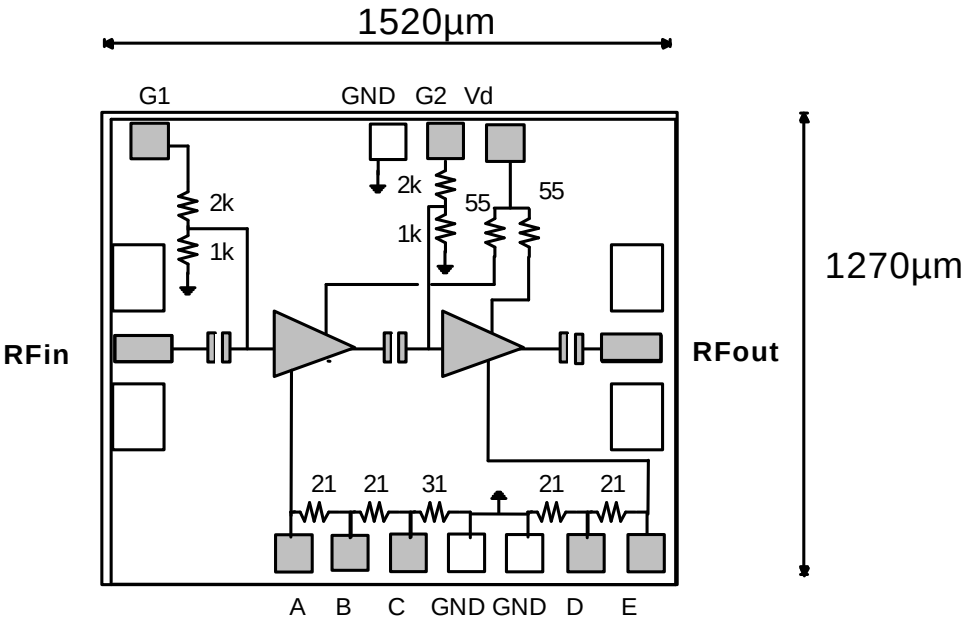
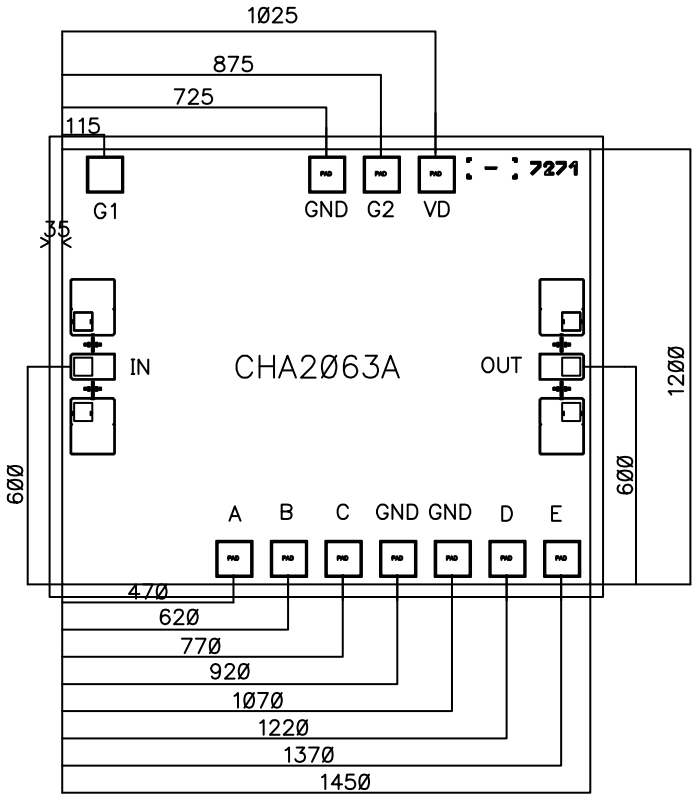
Mechanical data



Chip thickness: 100µm.
Chip size: 1270x1520 ±35µm
All dimensions are in micrometers

PAD location



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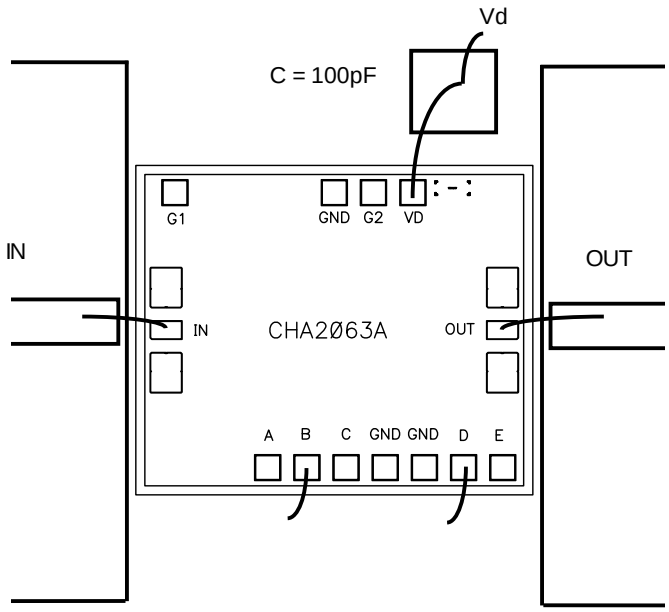
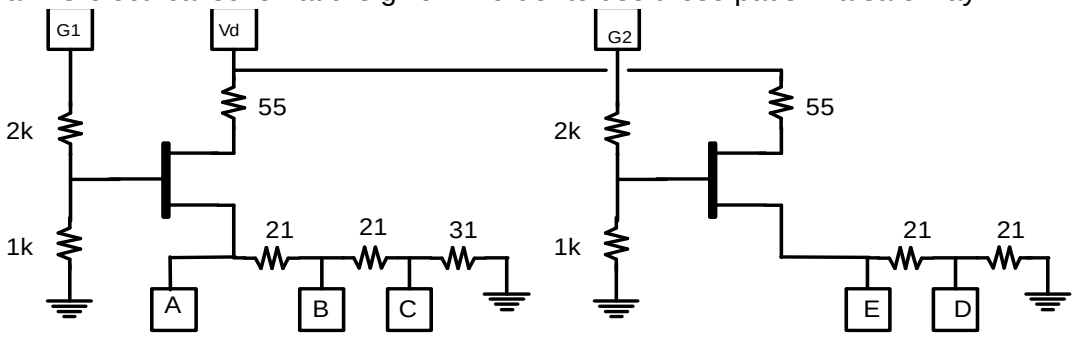
Recommended assembly plan



Note: Supply feed should be bypassed. 25µm diameter gold wire is to be preferred.

Chip Biasing options

This chip is self-biased, and flexibility is provided by the access to number of pads. the internal DC electrical schematic is given in order to use these pads in a safe way.



The two requirements are :
N°1 : Not exceed Vds = 3.5Volt (internal Drain to Source voltage).
N°2 : Biased in such a way to limit Vgs positive value (internal Gate to Source voltage).

We propose two standard biasing :

Low Noise and low consumption : Vd = 4V and B & D grounded.
All the other pads non connected (NC).
Idd = 40mA & Pout-1dB = +8dBm Typical.
(Equivalent to A,B,C,D,E : NC and Vd=4V ; G1=+2.5V ; G2=+2.5V).

Low Noise and high output power : Vd = 5V and B & E grounded.
All the other pads non connected (NC).
Idd = 75mA & Pout-1dB = +13dBm Typical.
(Equivalent to A,B,C,D,E : NC and Vd=5V ; G1=+2.5V ; G2=+1.0V).

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Notes

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Recommended ESD management

Refer to the application note AN0020 available at http://www.ums-gaas.com for ESD sensitivity and handling recommendations for the UMS products.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at http://www.ums-gaas.com.

Ordering Information

Chip form:	CHA2063a99F/00

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