±15 kV ESD Protected, Slew Rate Limited, 5 V, RS-485 Transceiver

ADM483E

FEATURES

±15 kV ESD protection
250 kbps data rate
Reduced slew rate for low EM interference
Single 5 V ± 10% supply
−7 V to +12 V bus common-mode range
Up to 32 nodes on the bus
Receiver open-circuit, fail-safe design
Short-circuit protection
36 µA supply current
0.1 µA shutdown current

APPLICATIONS

Low power RS-485 systems
Electrically harsh environments
EMI sensitive applications
DTE-DCE interface
Packet switching
Local area networks

FUNCTIONAL BLOCK DIAGRAM

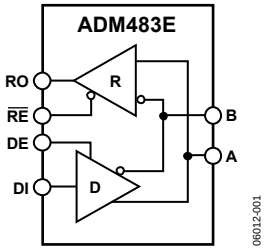

Figure 1.

GENERAL DESCRIPTION

The ADM483E is a 5 V, low power data transceiver with ±15 kV ESD protection suitable for half-duplex communication on multipoint bus transmission lines. The ADM483E is designed for balanced data transmission and complies with TIA/EIA Standards RS-485 and RS-422, which allow up to 32 transceivers on a bus.

The ADM483E has a low current shutdown mode in which it consumes only 0.1 µA.

Because only one driver is enabled at any time, the output of a disabled or power-down driver is three-stated to avoid overloading the bus.

Drivers are short-circuit current-limited and are protected against excessive power dissipation by thermal shutdown circuitry that places their outputs into a high impedance state. The receiver input has a fail-safe feature that guarantees a logic high output if the input is open circuit.

The ADM483E is fully specified over the industrial temperature ranges and is available in 8-lead SOIC_N packages.

Rev. A

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1/97—Revision 0: Initial Version

SPECIFICATIONS

V_{CC} = 5 V ± 10%. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DRIVER					
Differential Output Voltage, V_{OD}			5.0	V	V_{CC} = 5.25 V; R = ∞, see Figure 15
	2.0		5.0	V	R = 50 Ω (RS-422), see Figure 15
	1.5		5.0	V	R = 27 Ω (RS-485), see Figure 15
	1.5		5.0	V	V_{IN} = −7 V to +12 V
Δ|V_{OD}| for Complementary Output States			0.2	V	R = 27 Ω or 50 Ω, see Figure 15
Common-Mode Output Voltage, V_{OC}			3	V	R = 27 Ω or 50 Ω, see Figure 15
Δ|V_{OC}| for Complementary Output States			0.2	V	R = 27 Ω or 50 Ω
Output Short-Circuit Current (V_{OUT} = High)			250	mA	−7 V ≤ V_O ≤ +12 V
Output Short-Circuit Current (V_{OUT} = Low)			250	mA	−7 V ≤ V_O ≤ +12 V
CMOS Input Logic Threshold Low, V_{INL}		1.4	0.8	V	
CMOS Input Logic Threshold High, V_{INH}	2.0	1.4		V	
Logic Input Current (DE, DI)			±1.0	μA	
RECEIVER					
Differential Input Threshold Voltage, V_{TH}	−0.2		+0.2	V	−7 V ≤ V_{CM} ≤ +12 V
Input Voltage Hysteresis, ΔV_{TH}		70		mV	V_{CM} = 0 V
Input Resistance	12			kΩ	−7 V ≤ V_{CM} ≤ +12 V
Input Current (A, B)			1	mA	V_{IN} = 12 V
	−0.8			mA	V_{IN} = −7 V
Logic Enable Input Current ($\overline{RE}$)			±1	μA	
CMOS Output Voltage Low, V_{OL}			0.4	V	I_{OUT} = 4.0 mA
CMOS Output Voltage High, V_{OH}	4.0			V	I_{OUT} = −4.0 mA
Short-Circuit Output Current	7		85	mA	V_{OUT} = GND or V_{CC}
Three-State Output Leakage Current			±2.0	μA	0.4 V ≤ V_{OUT} ≤ 2.4 V
POWER SUPPLY CURRENT					Outputs unloaded, receivers enabled
I_{CC}		36	120	μA	DE = 0 V (disabled), $\overline{RE}$ = 0 V
		270	360	μA	DE = 5 V (enabled), $\overline{RE}$ = 0 V
Supply Current in Shutdown		0.1	10	μA	DE = 0 V, $\overline{RE}$ = V_{CC}
ESD IMMUNITY					
ESD Protection		±15		kV	HBM air discharge; Pin A, Pin B

TIMING SPECIFICATIONS

V_{CC} = 5 V ± 10%. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DRIVER					
Propagation Delay Input to Output (t_{PLH}, t_{PHL})	250		2000	ns	R_L Diff = 54 Ω, C_{L1} = C_{L2} = 100 pF, see Figure 16 and Figure 17
Driver Output to $\overline{\text{Output}}$ (t_{SKEW})		100	800	ns	R_L Diff = 54 Ω, C_{L1} = C_{L2} = 100 pF, see Figure 16 and Figure 17
Driver Rise/Fall Time (t_R, t_F)	250		2000	ns	R_L Diff = 54 Ω, C_{L1} = C_{L2} = 100 pF, see Figure 16 and Figure 17
Driver Enable to Output Valid	250		2000	ns	R_L = 500 Ω, C_L = 100 pF, see Figure 18 and Figure 19
Driver Disable Timing	300		3000	ns	R_L = 500 Ω, C_L = 15 pF, see Figure 18 and Figure 19
RECEIVER					
Propagation Delay Input to Output (t_{PLH}, t_{PHL})	250		2000	ns	C_L = 15 pF, see Figure 20
Skew ($\lvert t_{PLH} - t_{PHL} \rvert$)		200		ns	
Receiver Enable (t_{EN1})		10	50	ns	R_L = 1 kΩ, C_L = 15 pF, see Figure 22
Receiver Disable (t_{EN2})		10	50	ns	R_L = 1 kΩ, C_L = 15 pF, see Figure 22
SHUTDOWN					
Time to Shutdown	50	200	3000	ns	
Driver Enable from Shutdown			5000	ns	R_L = 500 Ω, C_L = 100 pF, see Figure 18 and Figure 19
Receiver Enable from Shutdown			5000	ns	R_L = 1 kΩ, C_L = 15 pF, see Figure 22

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
V_{CC} to GND	−0.5 V to +6 V
Digital I/O Voltage (DE, $\overline{RE}$)	−0.5 V to (V_{CC} + 0.5 V)
Driver Input Voltage (DI)	−0.5 V to (V_{CC} + 0.5 V)
Receiver Output Voltage (RO)	−0.5 V to (V_{CC} + 0.5 V)
Driver Output/Receiver Input Voltage (Pin A, Pin B)	−9 V to +14 V
ESD Rating: Air (Human Body Model) (Pin A, Pin B)	±15 kV
Power Dissipation 8-Lead SOIC_N	470 mW
θ_{JA}, Thermal Impedance	110°C/W
Operating Temperature Range	
Industrial (A Version)	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

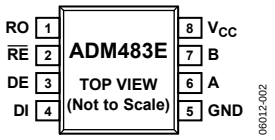


Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	RO	Receiver Output. When enabled, if A > B by 200 mV, then RO = high. If A < B by 200 mV, then RO = low.
2	$\overline{RE}$	Receiver Output Enable. A low level enables the receiver output, RO. A high level places the receiver output in a high impedance state.
3	DE	Driver Output Enable. A high level enables the driver differential outputs, A and B. A low level places the driver differential outputs in a high impedance state.
4	DI	Driver Input. When the driver is enabled, a logic low on DI forces A low and B high. A logic high on DI forces A high and B low.
5	GND	Ground Connection, 0 V.
6	A	Noninverting Receiver Input A/Driver Output A.
7	B	Inverting Receiver Input B/Driver Output B.
8	V_{CC}	Power Supply, 5 V ± 10%.

Table 5. Selection Table

Part No.	Duplex	Data Rate (kbps)	Low Power Shutdown	Tx/Rx Enable	I_{CC} (µA)	No. of Tx/Rx on Bus	ESD kV
ADM483E	Half	250	Yes	Yes	36	32	±15

TYPICAL PERFORMANCE CHARACTERISTICS

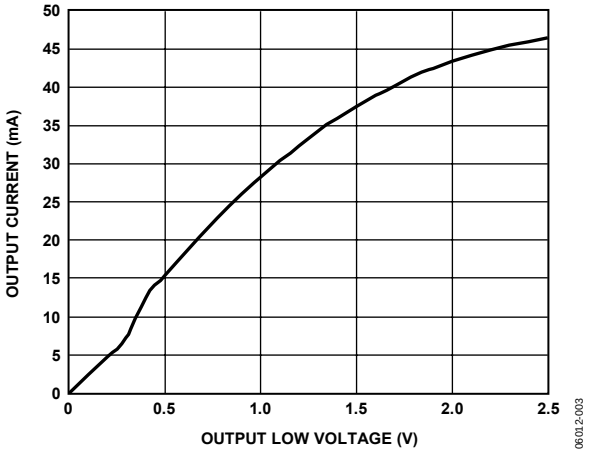


Figure 3. Output Current vs. Receiver Output Low Voltage

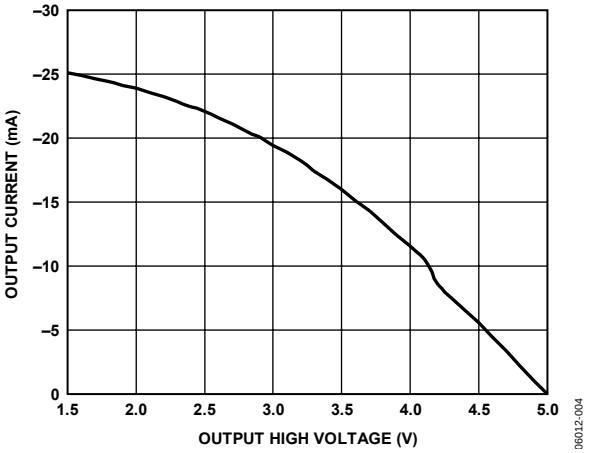


Figure 4. Output Current vs. Receiver Output High Voltage

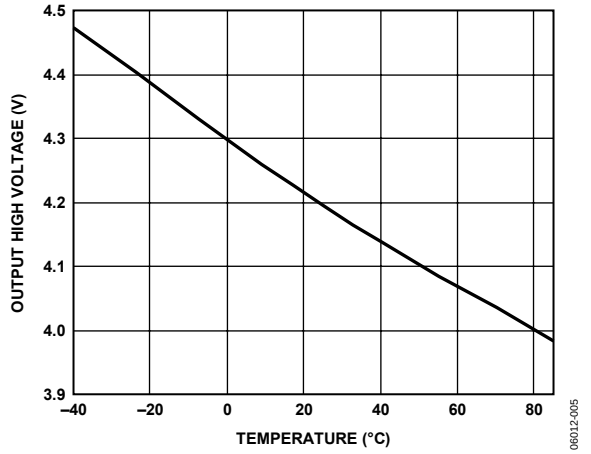


Figure 5. Receiver Output High Voltage vs. Temperature

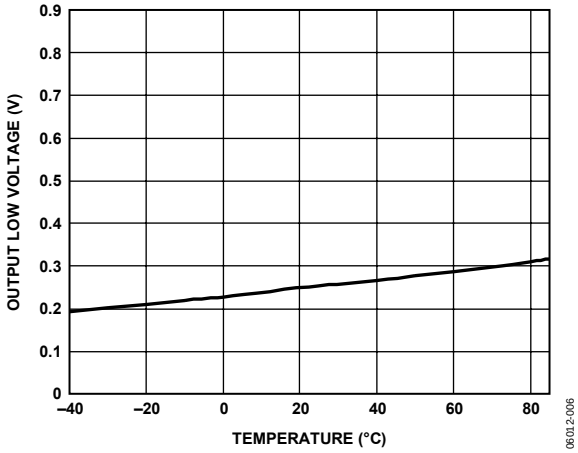


Figure 6. Receiver Output Low Voltage vs. Temperature

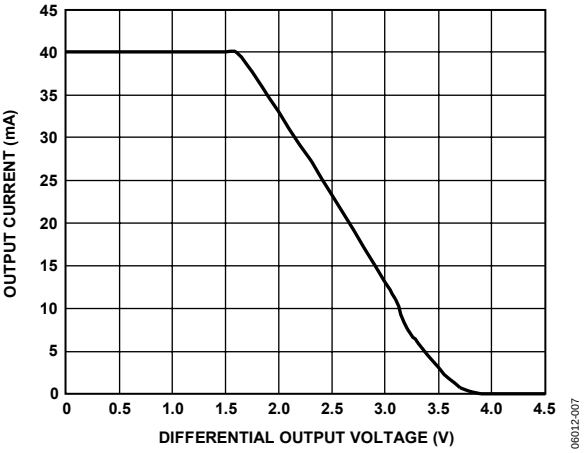


Figure 7. Driver Output Current vs. Differential Output Voltage

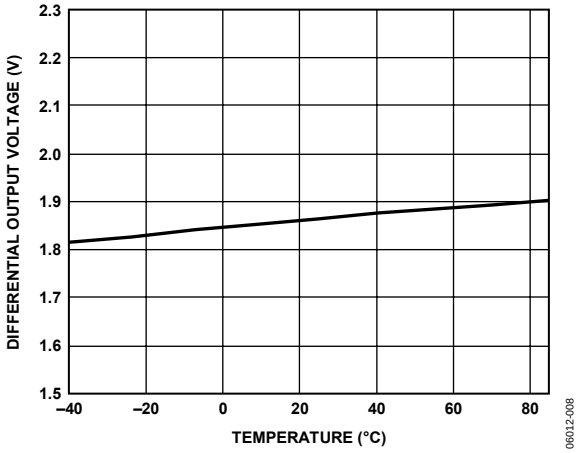


Figure 8. Driver Differential Output Voltage vs. Temperature

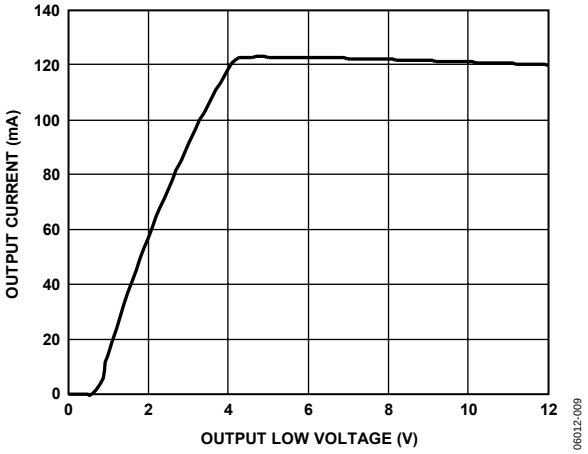


Figure 9. Output Current vs. Driver Output Low Voltage

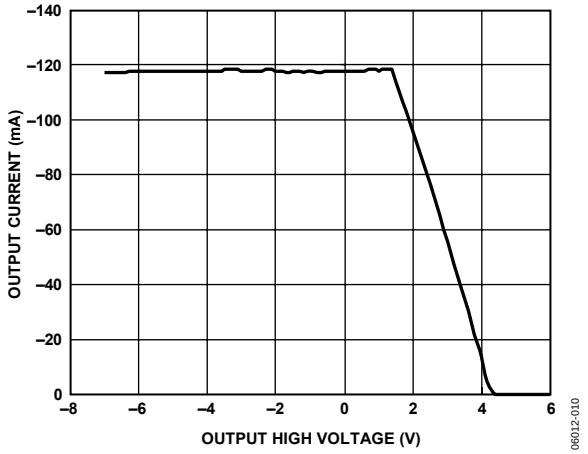


Figure 10. Output Current vs. Driver Output High Voltage

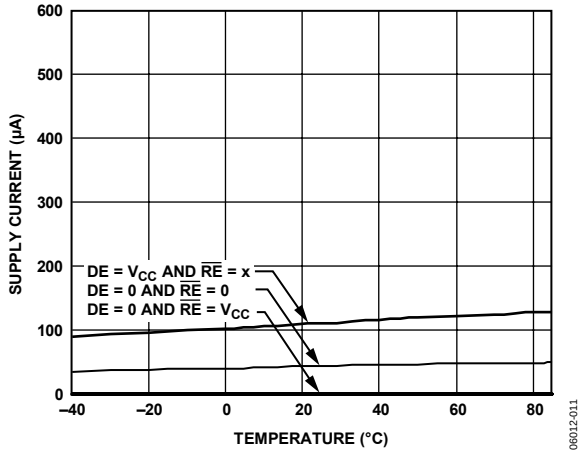


Figure 11. ADM483E Supply Current vs. Temperature

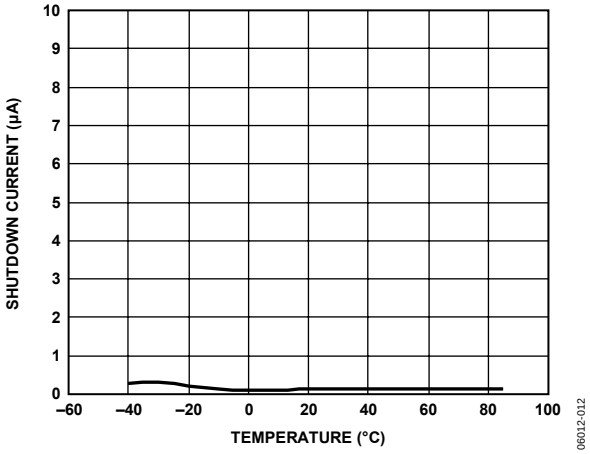


Figure 12. Shutdown Current vs. Temperature

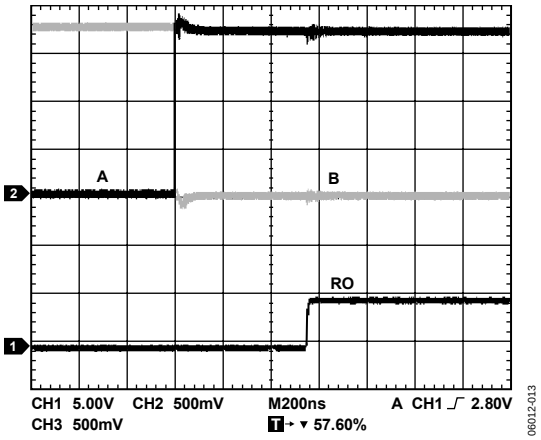


Figure 13. ADM483E Receiver t_{PHL}

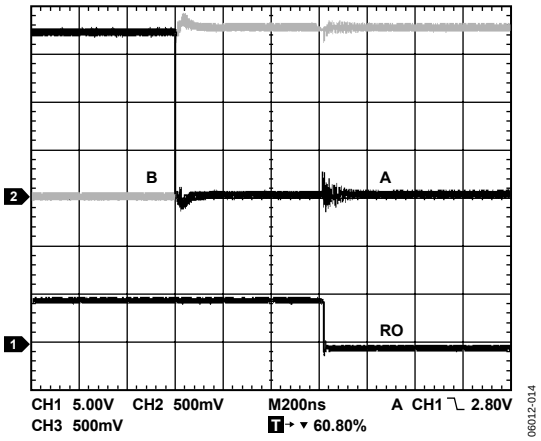


Figure 14. ADM483E Receiver t_{PLH} Driven by External RS-485 Device

TEST CIRCUITS AND SWITCHING CHARACTERISTICS

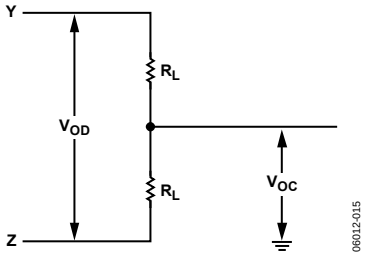


Figure 15. Driver DC Test Load

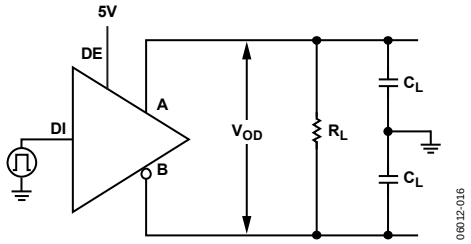


Figure 16. Driver Timing Test Circuit

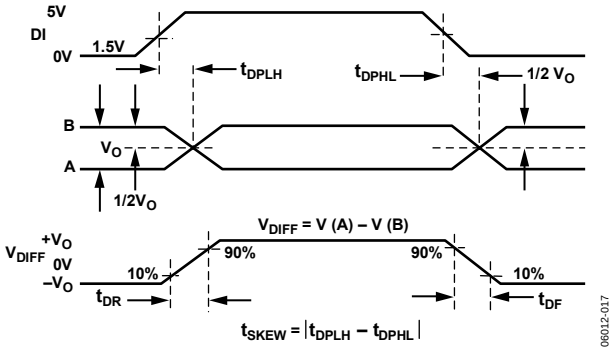


Figure 17. Driver Propagation Delays

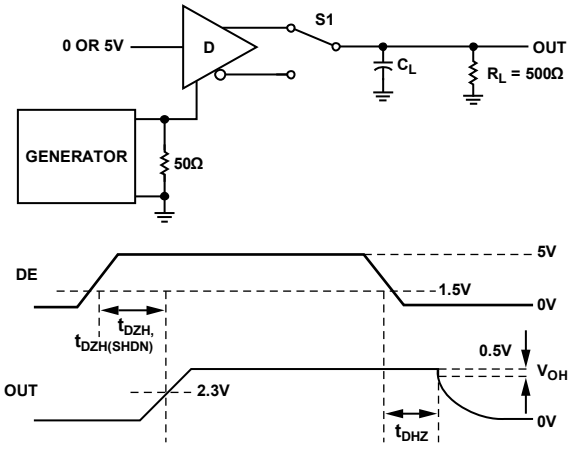
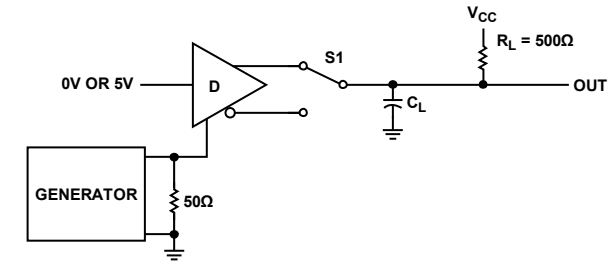


Figure 18. Driver Enable and Disable Times (t_{DHZ}, t_{DZH}, $t_{DZH(SHDN)}$)



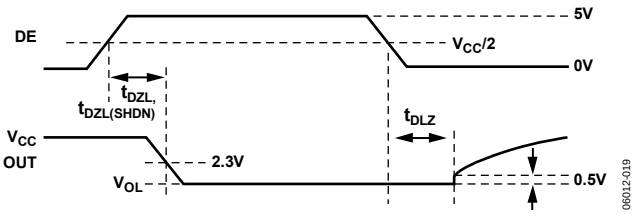


Figure 19. Driver Enable and Disable Times (t_{DZL}, t_{DLZ}, $t_{DZL(SHDN)}$)

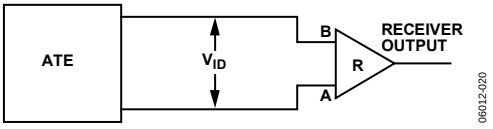


Figure 20. Receiver Propagation Delay Test Circuit

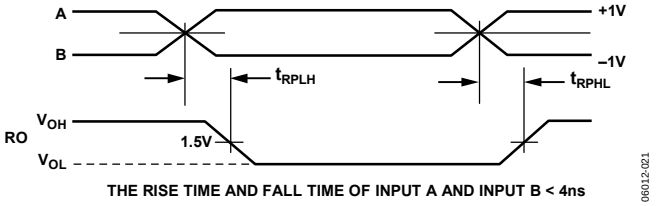


Figure 21. Receiver Propagation Delays

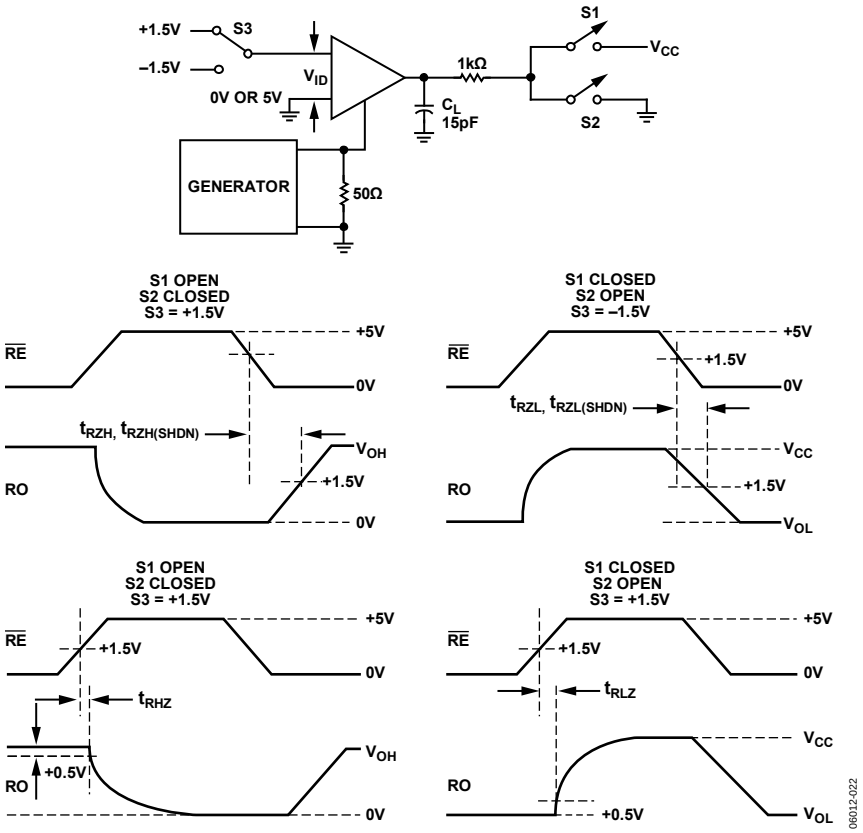


Figure 22. Receiver Enable and Disable Times

GENERAL INFORMATION

The ADM483E is a robust RS-485 transceiver that operates from a single 5 V supply.

It is ideally suited for operation in electrically harsh environments or where cables may be plugged and unplugged. It is also immune to high RF field strengths without special shielding precautions. The ADM483E is intended for balanced data transmission and complies with both EIA Standards RS-485 and RS-422. It contains a differential line driver and a differential line receiver; it is suitable for half-duplex data transmission because the driver and receiver share the same differential pins.

The input impedance on the ADM483E is 12 kΩ, allowing up to 32 transceivers on the differential bus.

The ADM483E operates from a single 5 V ± 10% power supply. Excessive power dissipation caused by bus contention or by output shorting is prevented by a thermal shutdown circuit. This feature forces the driver output into a high impedance state if, during fault conditions, a significant temperature increase is detected in the internal driver circuitry.

The receiver has a fail-safe feature that results in a logic high output state if the inputs are unconnected (floating).

A high level of robustness is achieved using internal protection circuitry, eliminating the need for external protection components such as transorbs or surge suppressors.

Low electromagnetic emissions are achieved using slew limited drivers, minimizing interference both conducted and radiated.

The ADM483E can transmit at data rates up to 250 kbps.

A typical application for the ADM483E is illustrated in Figure 23. This figure shows a half-duplex link where data may be transferred at rates up to 250 kbps. A terminating resistor is shown at both ends of the link. This termination is not critical because the slew rate is controlled by the ADM483E and reflections are minimized.

The communications network can be extended to include multipoint connections as shown in Figure 26. Up to 32 transceivers can be connected to the bus.

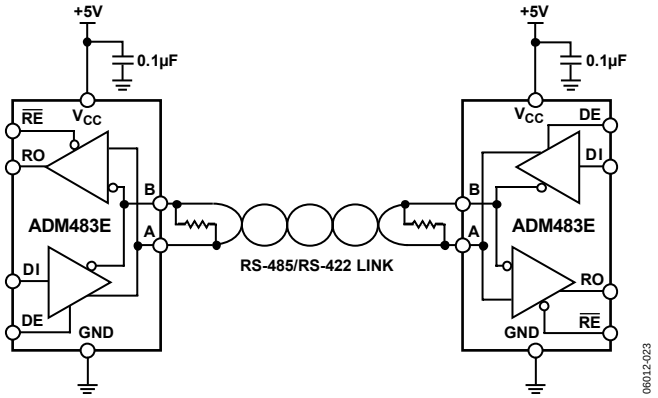


Figure 23. Typical Half-Duplex Link Application

Table 6 and Table 7 show the truth tables for transmitting and receiving.

Table 6. Transmitting Truth Table

Inputs			Outputs	
$\overline{RE}$	DE	DI	B	A
X[1]	1	1	0	1
X[1]	1	0	1	0
0	0	X[1]	High-Z	High-Z
1	0	X[1]	High-Z	High-Z

[1] X = don't care.

Table 7. Receiving Truth Table

Inputs		Outputs	
$\overline{RE}$	DE	A – B	RO
0	0	≥ +0.2 V	1
0	0	≤ −0.2 V	0
0	0	Inputs O/C	1
1	0	X[1]	High-Z

[1] X = don't care.

ESD TRANSIENT PROTECTION SCHEME

The ADM483E uses protective clamping structures on its inputs and outputs that clamp the voltage to a safe level and dissipate the energy present in ESD (electrostatic discharge).

The protection structure achieves ESD protection up to ±15 kV according to the Human Body Model.

ESD TESTING

Two coupling methods are used for ESD testing: contact discharge and air-gap discharge. Contact discharge calls for a direct connection to the unit being tested. Air-gap discharge uses a higher test voltage but does not make direct contact with the unit under test. With air-gap discharge, the discharge gun is moved toward the unit under test, developing an arc across the air gap. This method is influenced by humidity, temperature, barometric pressure, distance, and rate of closure of the discharge gun. The contact discharge method, though less realistic, is more repeatable and is gaining acceptance and preference over the air-gap method.

Although very little energy is contained within an ESD pulse, the extremely fast rise time, coupled with high voltages, can cause failures in unprotected semiconductors. Catastrophic destruction may occur immediately as a result of arcing or heating. Even if catastrophic failure does not occur immediately, the device may suffer from parametric degradation, which can result in degraded performance. The cumulative effects of continuous exposure may eventually lead to complete failure.

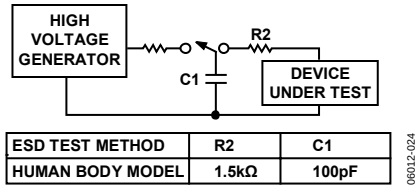


Figure 24. ESD Generator

I/O lines are particularly vulnerable to ESD damage. Simply touching or plugging in an I/O cable can result in a static discharge that may damage or completely destroy the interface product connected to the I/O port.

It is, therefore, extremely important to have high levels of ESD protection on the I/O lines.

It is possible that the ESD discharge could induce latch-up in the device under test. Therefore, it is important that ESD testing on the I/O pins be carried out while device power is applied. This type of testing is more representative of a real-world I/O discharge where the equipment is operating normally when the discharge occurs.

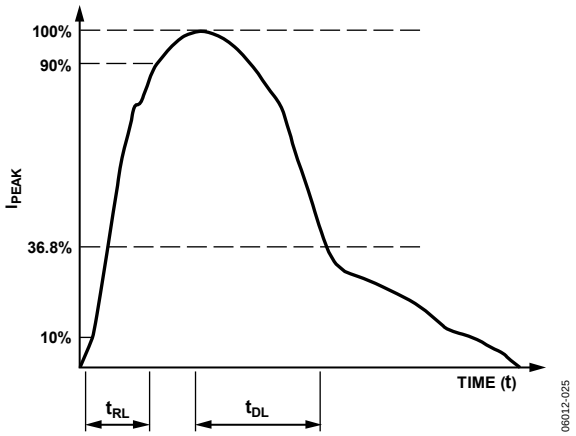


Figure 25. Human Body Model ESD Current Waveform

Table 8. ADM483E ESD Test Results

ESD Test Method	I/O Pins
Human Body Model: Air	±15 kV
Human Body Model: Contact	±8 kV

APPLICATIONS INFORMATION

DIFFERENTIAL DATA TRANSMISSION

Differential data transmission is used to reliably transmit data at high rates over long distances and through noisy environments. Differential transmission nullifies the effects of ground shifts and noise signals that appear as common-mode voltages on the line. There are two main standards approved by the Electronics Industries Association (EIA) that specify the electrical characteristics of transceivers used in differential data transmission.

The RS-422 standard specifies data rates up to 10 MBaud and line lengths up to 4000 feet. A single driver can drive a transmission line with up to 10 receivers.

To accommodate true multipoint communications, the RS-485 standard was defined. This standard meets or exceeds all the requirements of RS-422 and also allows for up to 32 drivers and 32 receivers to be connected to a single bus. An extended common-mode range of −7 V to +12 V is defined. The most significant difference between RS-422 and RS-485 is the fact that the drivers can be disabled, thereby allowing more than one (32, in fact) to be connected to a single line. Only one driver should be enabled at a time, but the RS-485 standard contains additional specifications to guarantee device safety in the event of line contention.

CABLE AND DATA RATE

The transmission line of choice for RS-485 communications is a twisted pair. Twisted pair cable tends to cancel common-mode noise and also cancels the magnetic fields generated by the current flowing through each wire, thereby reducing the effective inductance of the pair.

A typical application showing a multipoint transmission network is shown in Figure 26. An RS-485 transmission line can have as many as 32 transceivers on the bus. Only one driver can transmit at a particular time, but multiple receivers can be enabled simultaneously.

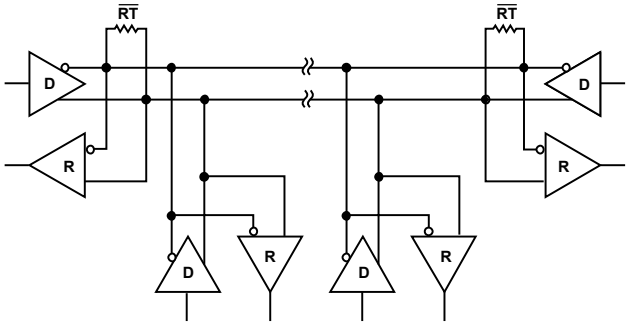


Figure 26. Typical RS-485 Network

OUTLINE DIMENSIONS

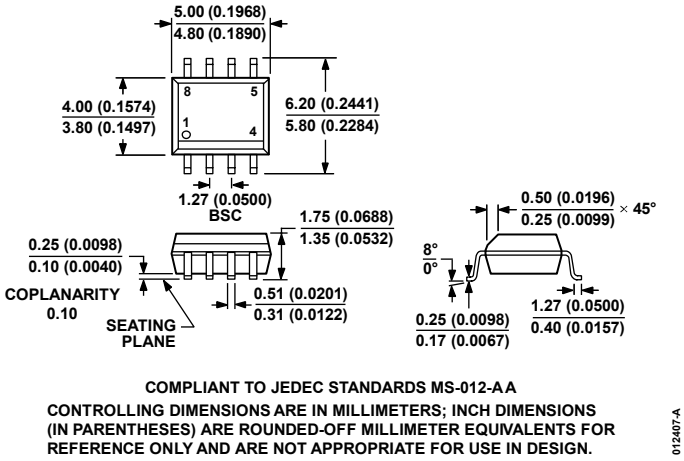


Figure 27. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Ordering Quantity
ADM483EAR	–40°C to +85°C	8-Lead Standard Small Outline Package (SOIC_N)	R-8	
ADM483EAR-REEL	–40°C to +85°C	8-Lead Standard Small Outline Package (SOIC_N)	R-8	2500
ADM483EARZ[1]	–40°C to +85°C	8-Lead Standard Small Outline Package (SOIC_N)	R-8	
ADM483EARZ-REEL[1]	–40°C to +85°C	8-Lead Standard Small Outline Package (SOIC_N)	R-8	2500

[1]Z = RoHS Compliant Part.

NOTES

NOTES

D06012-0-12/07(A)

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