

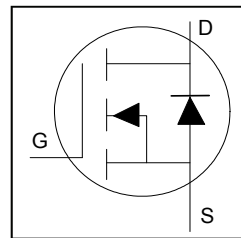
**Application**

- Brushed motor drive applications
- BLDC motor drive applications
- Battery powered circuits
- Half-bridge and full-bridge topologies
- Synchronous rectifier applications
- Resonant mode power supplies
- OR-ing and redundant power switches
- DC/DC and AC/DC converters
- DC/AC inverters

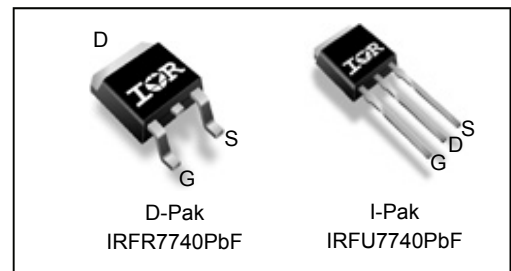
**Benefits**

- Improved gate, avalanche and dynamic dV/dt ruggedness
- Fully characterized capacitance and avalanche SOA
- Enhanced body diode dV/dt and dI/dt capability
- Lead-free, RoHS compliant

HEXFET® Power MOSFET

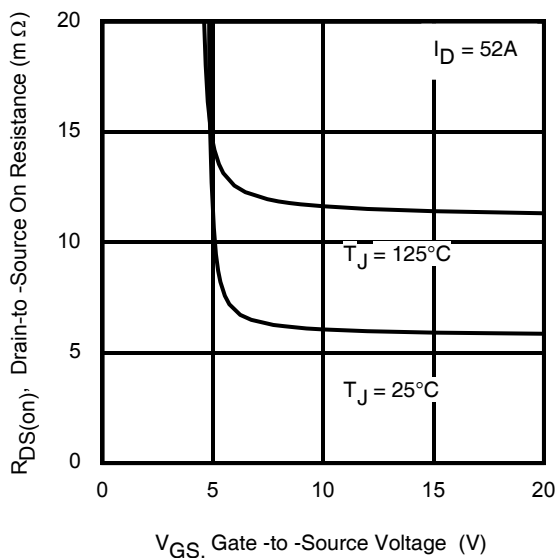


<b>V<sub>DSS</sub></b>	<b>75V</b>
<b>R<sub>DS(on)</sub> typ.</b>	<b>6.0mΩ</b>
	<b>max</b>
<b>I<sub>D</sub></b>	<b>87A</b>

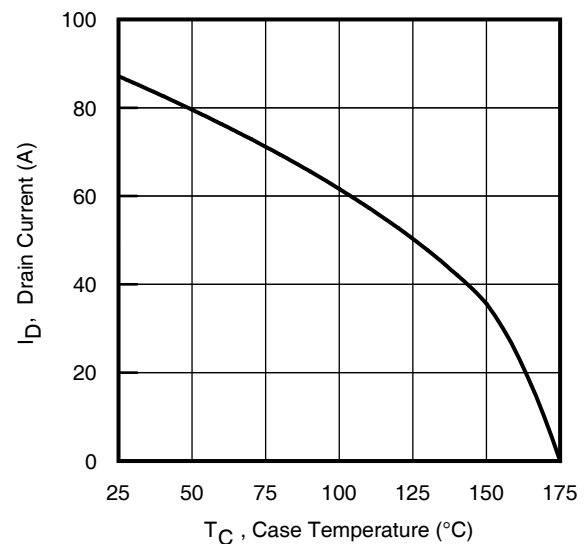


<b>G</b>	<b>D</b>	<b>S</b>
Gate	Drain	Source

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRFR7740PbF	D-Pak	Tube	75	IRFR7740PbF
		Tape and Reel	2000	IRFR7740TRPbF
IRFU7740PbF	I-Pak	Tube	75	IRFU7740PbF



**Fig 1.** Typical On-Resistance vs. Gate Voltage



**Fig 2.** Maximum Drain Current vs. Case Temperature

**Absolute Maximum Rating**

Symbol	Parameter	Max.	Units
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Silicon Limited)	87	A
$I_D @ T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Silicon Limited)	62	
$I_{DM}$	Pulsed Drain Current ①	330	
$P_D @ T_C = 25^\circ\text{C}$	Maximum Power Dissipation	140	W
	Linear Derating Factor	0.95	W/°C
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
$T_J$ $T_{STG}$	Operating Junction and Storage Temperature Range	-55 to +175	°C
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	

**Avalanche Characteristics**

Symbol	Parameter	Max.	Units
$E_{AS}$ (Thermally limited)	Single Pulse Avalanche Energy ②	160	mJ
$E_{AS}$ (Thermally limited)	Single Pulse Avalanche Energy ③	242	
$I_{AR}$	Avalanche Current ④	See Fig 15, 16, 23a, 23b	A
$E_{AR}$	Repetitive Avalanche Energy ⑤		mJ

**Thermal Resistance**

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑦	—	1.05	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount) ⑧	—	50	
$R_{\theta JA}$	Junction-to-Ambient	—	110	

**Static @  $T_J = 25^\circ\text{C}$  (unless otherwise specified)**

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	75	—	—	V	$V_{GS} = 0\text{V}, I_D = 250\mu\text{A}$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	51	—	mV/°C	Reference to $25^\circ\text{C}, I_D = 1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	6.0	7.2	m $\Omega$	$V_{GS} = 10\text{V}, I_D = 52\text{A}$
		—	7.0	—		$V_{GS} = 6.0\text{V}, I_D = 26\text{A}$
$V_{GS(th)}$	Gate Threshold Voltage	2.1	—	3.7	V	$V_{DS} = V_{GS}, I_D = 100\mu\text{A}$
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	1.0	$\mu\text{A}$	$V_{DS} = 75\text{V}, V_{GS} = 0\text{V}$
		—	—	150		$V_{DS} = 75\text{V}, V_{GS} = 0\text{V}, T_J = 125^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20\text{V}$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20\text{V}$
$R_G$	Gate Resistance	—	2.2	—	$\Omega$	

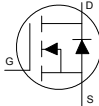
**Notes:**

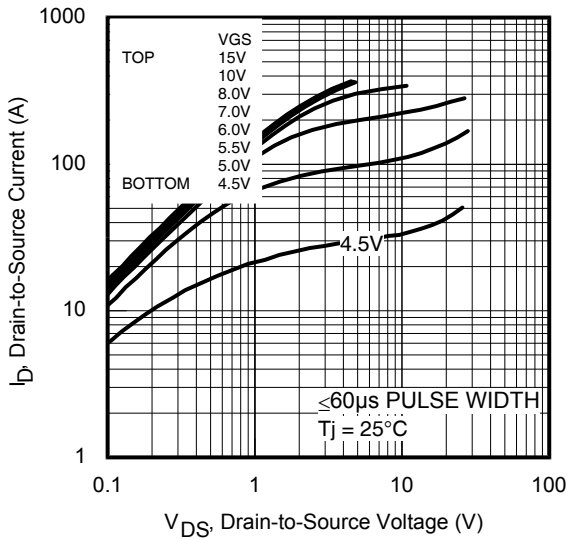
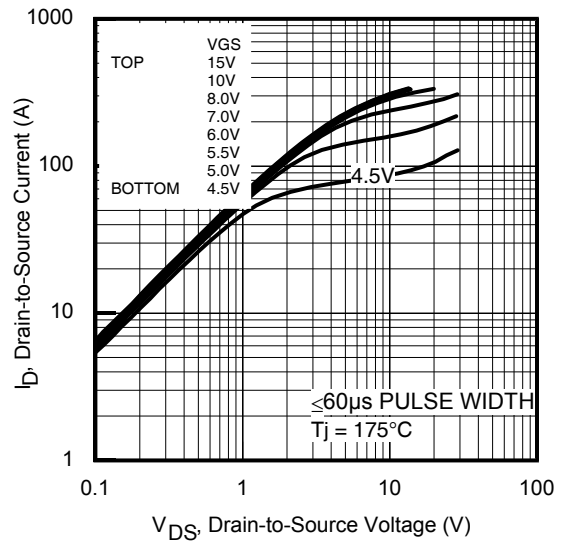
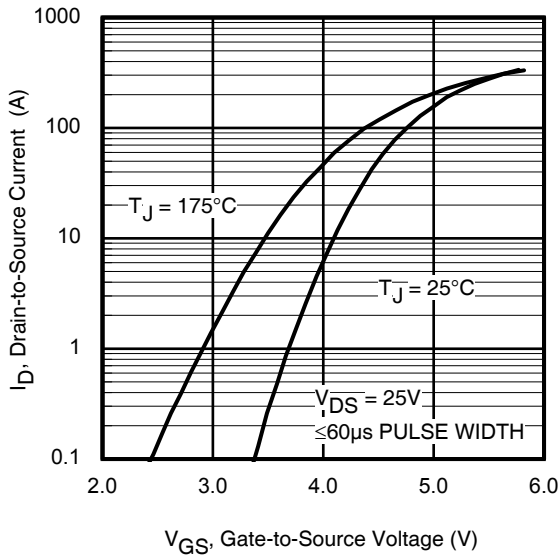
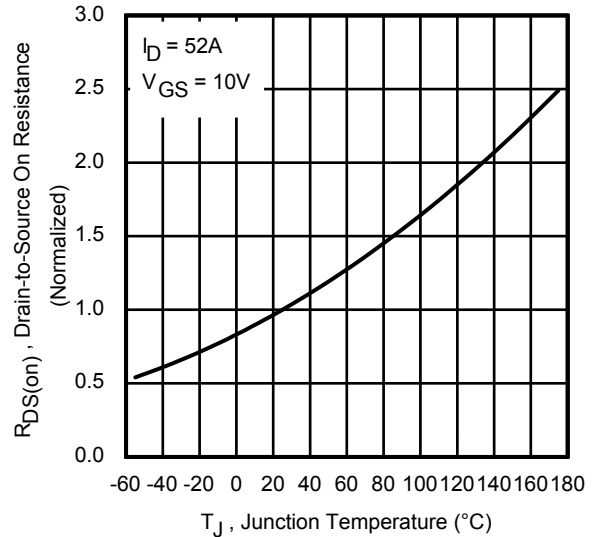
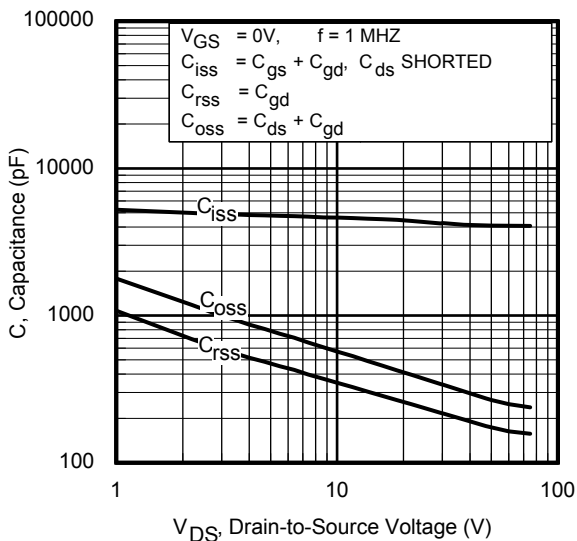
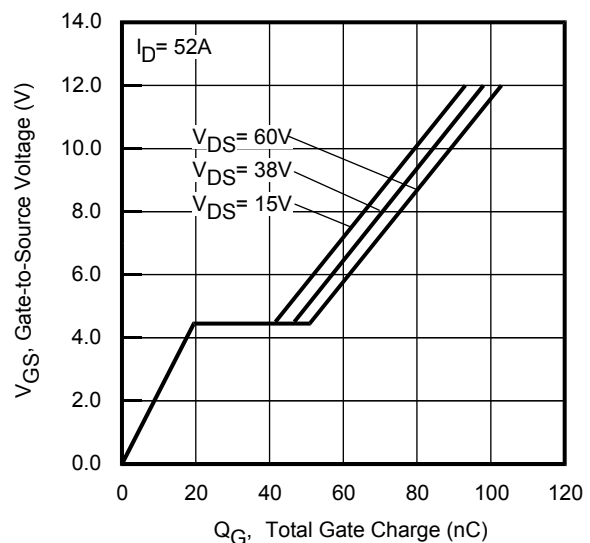
- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Limited by  $T_{Jmax}$ , starting  $T_J = 25^\circ\text{C}$ ,  $L = 120\mu\text{H}$ ,  $R_G = 50\Omega$ ,  $I_{AS} = 52\text{A}$ ,  $V_{GS} = 10\text{V}$ .
- ③  $I_{SD} \leq 52\text{A}$ ,  $di/dt \leq 570\text{A}/\mu\text{s}$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  $T_J \leq 175^\circ\text{C}$ .
- ④ Pulse width  $\leq 400\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- ⑤  $C_{oss}$  eff. (TR) is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .
- ⑥  $C_{oss}$  eff. (ER) is a fixed capacitance that gives the same energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .
- ⑦  $R_{\theta}$  is measured at  $T_J$  approximately  $90^\circ\text{C}$ .
- ⑧ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994: <http://www.irf.com/technical-info/appnotes/an-994.pdf>
- ⑨ Limited by  $T_{Jmax}$ , starting  $T_J = 25^\circ\text{C}$ ,  $L = 1\text{mH}$ ,  $R_G = 50\Omega$ ,  $I_{AS} = 22\text{A}$ ,  $V_{GS} = 10\text{V}$

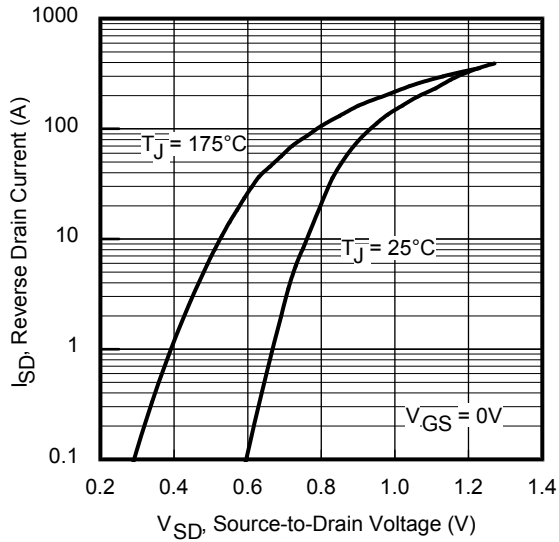
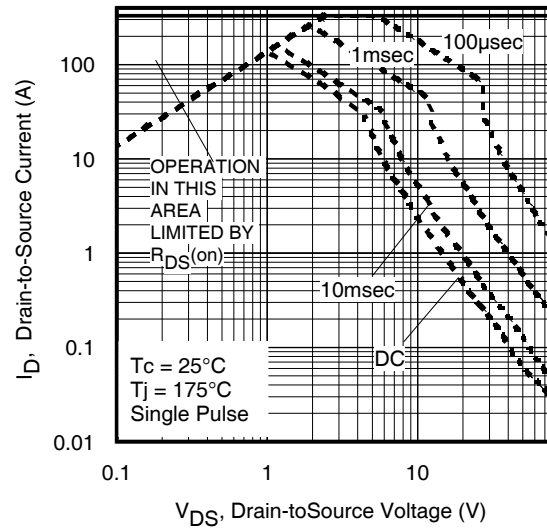
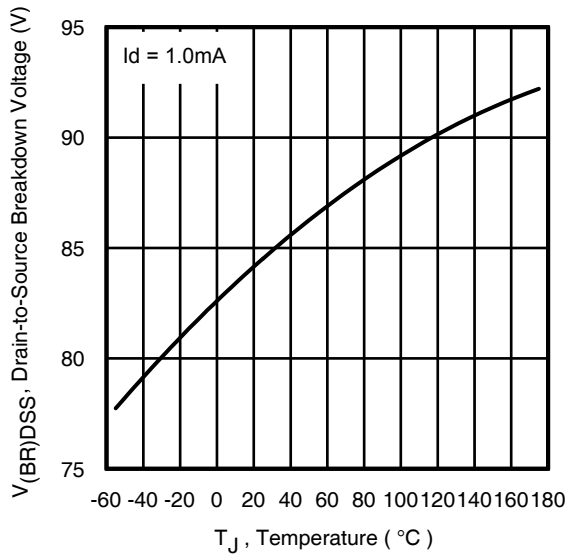
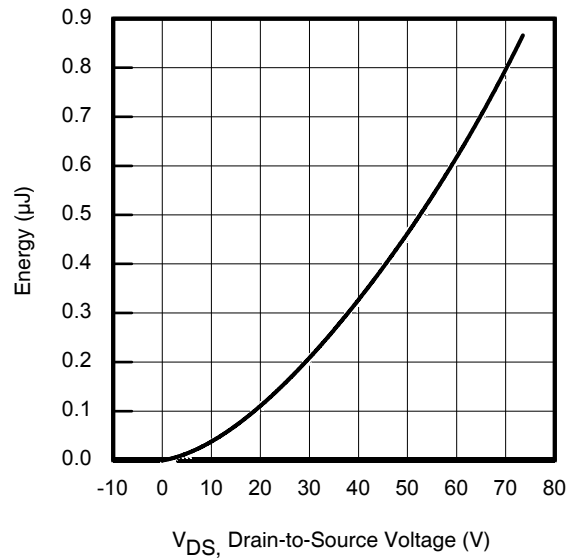
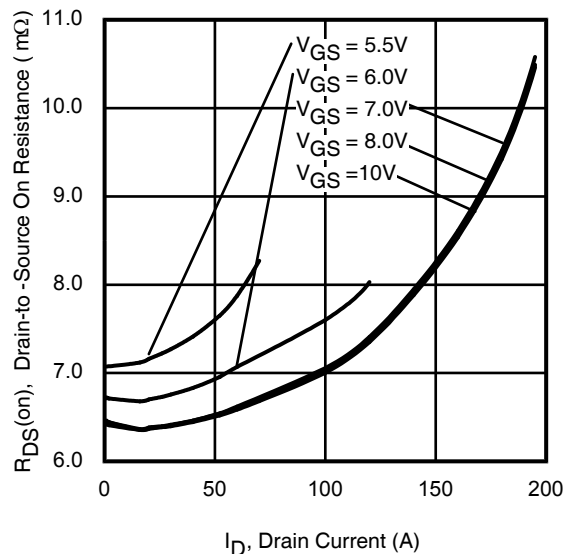
**Dynamic Electrical Characteristics @  $T_J = 25^\circ\text{C}$  (unless otherwise specified)**

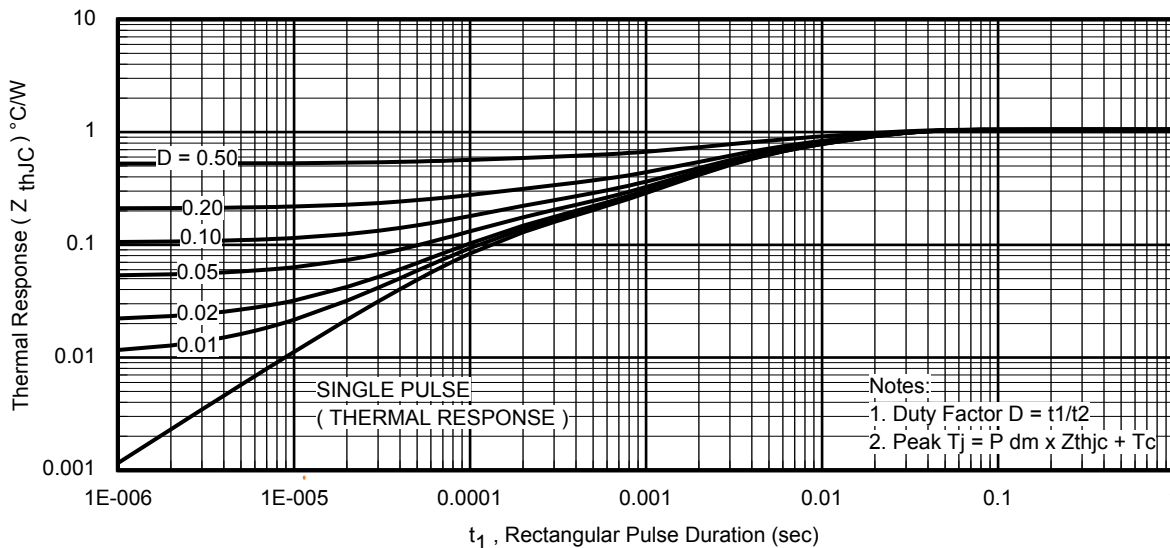
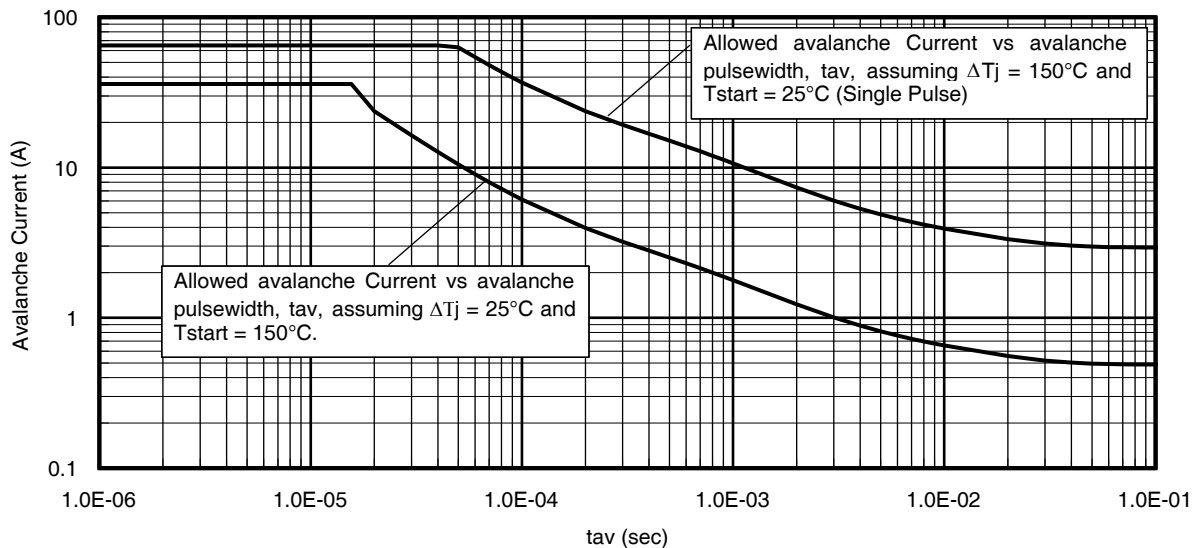
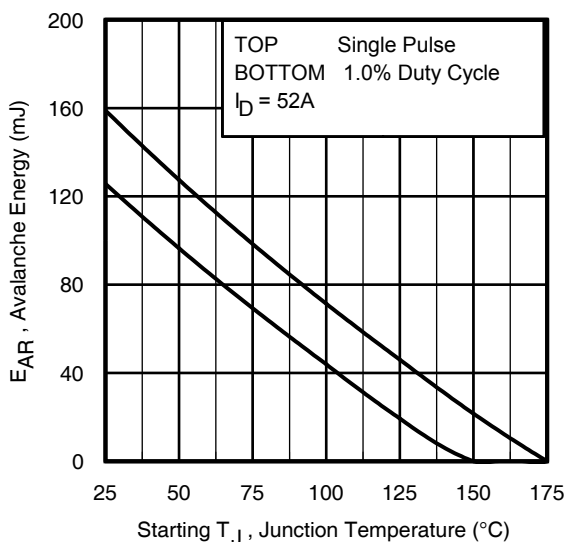
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
gfs	Forward Transconductance	110	—	—	S	$V_{DS} = 25\text{V}$ , $I_D = 52\text{A}$
$Q_g$	Total Gate Charge	—	84	126	nC	$I_D = 52\text{A}$ $V_{DS} = 38\text{V}$ $V_{GS} = 10\text{V}$ ④
$Q_{gs}$	Gate-to-Source Charge	—	20	—		
$Q_{gd}$	Gate-to-Drain Charge	—	26	—		
$Q_{sync}$	Total Gate Charge Sync. ( $Q_g - Q_{gd}$ )	—	58	—		
$t_{d(on)}$	Turn-On Delay Time	—	10	—	ns	$V_{DD} = 38\text{V}$ $I_D = 52\text{A}$ $R_G = 2.7\Omega$ $V_{GS} = 10\text{V}$ ④
$t_r$	Rise Time	—	36	—		
$t_{d(off)}$	Turn-Off Delay Time	—	55	—		
$t_f$	Fall Time	—	30	—		
$C_{iss}$	Input Capacitance	—	4430	—	pF	$V_{GS} = 0\text{V}$ $V_{DS} = 25\text{V}$ $f = 1.0\text{MHz}$ , See Fig.7 $V_{GS} = 0\text{V}$ , $V_{DS} = 0\text{V}$ to $60\text{V}$ ⑥ $V_{GS} = 0\text{V}$ , $V_{DS} = 0\text{V}$ to $60\text{V}$ ⑤
$C_{oss}$	Output Capacitance	—	370	—		
$C_{riss}$	Reverse Transfer Capacitance	—	230	—		
$C_{oss\text{ eff.}(ER)}$	Effective Output Capacitance (Energy Related)	—	340	—		
$C_{oss\text{ eff.}(TR)}$	Output Capacitance (Time Related)	—	440	—		

**Diode Characteristics**

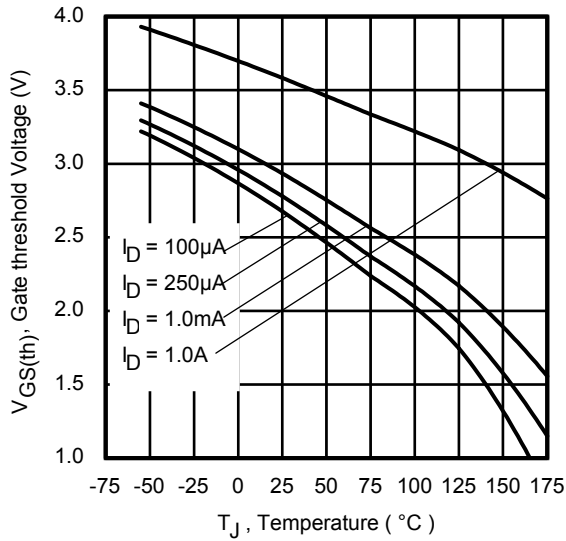
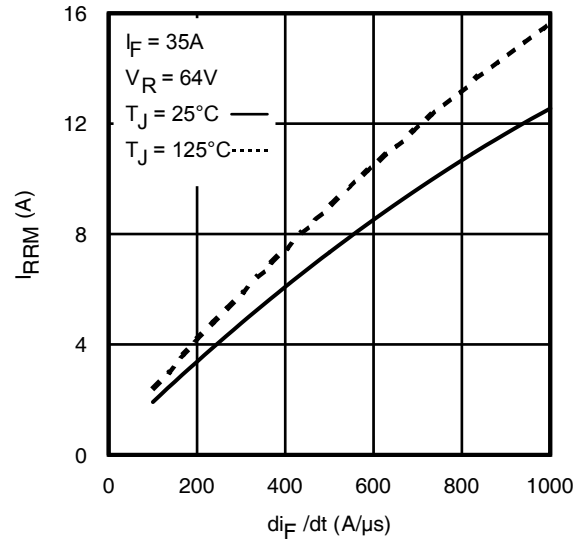
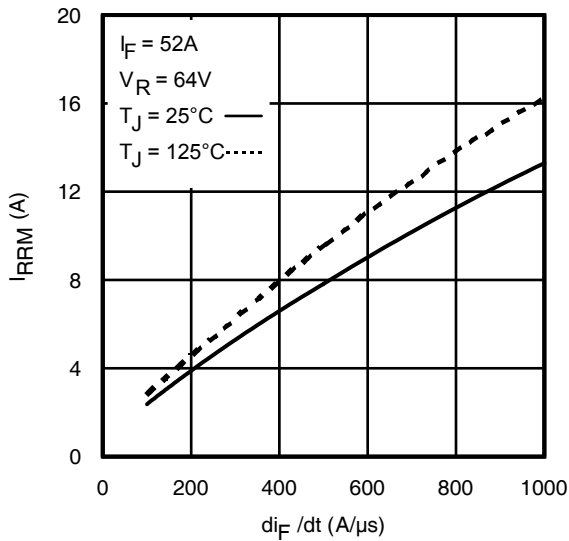
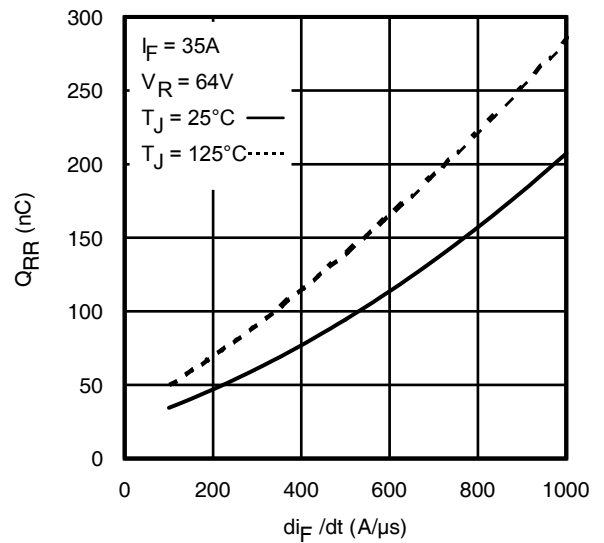
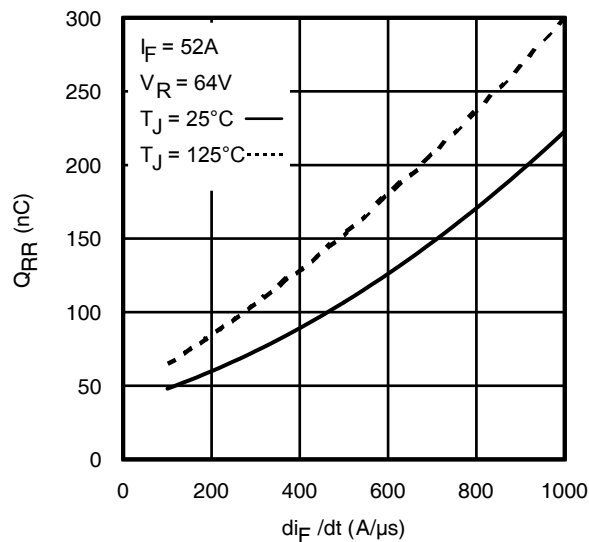
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	87	A	MOSFET symbol showing the integral reverse p-n junction diode. 
$I_{SM}$	Pulsed Source Current (Body Diode) ①	—	—	330		
$V_{SD}$	Diode Forward Voltage	—	—	1.2	V	$T_J = 25^\circ\text{C}$ , $I_S = 52\text{A}$ , $V_{GS} = 0\text{V}$ ④
dv/dt	Peak Diode Recovery dv/dt	—	12	—	V/ns	$T_J = 175^\circ\text{C}$ , $I_S = 52\text{A}$ , $V_{DS} = 75\text{V}$ ③
$t_{rr}$	Reverse Recovery Time	—	35	—	ns	$T_J = 25^\circ\text{C}$ $V_{DD} = 64\text{V}$ $T_J = 125^\circ\text{C}$ $I_F = 52\text{A}$ , $T_J = 25^\circ\text{C}$ $di/dt = 100\text{A}/\mu\text{s}$ ④ $T_J = 125^\circ\text{C}$
		—	40	—		
$Q_{rr}$	Reverse Recovery Charge	—	45	—	nC	$T_J = 25^\circ\text{C}$ $T_J = 125^\circ\text{C}$
		—	61	—		
$I_{RRM}$	Reverse Recovery Current	—	2.3	—	A	$T_J = 25^\circ\text{C}$

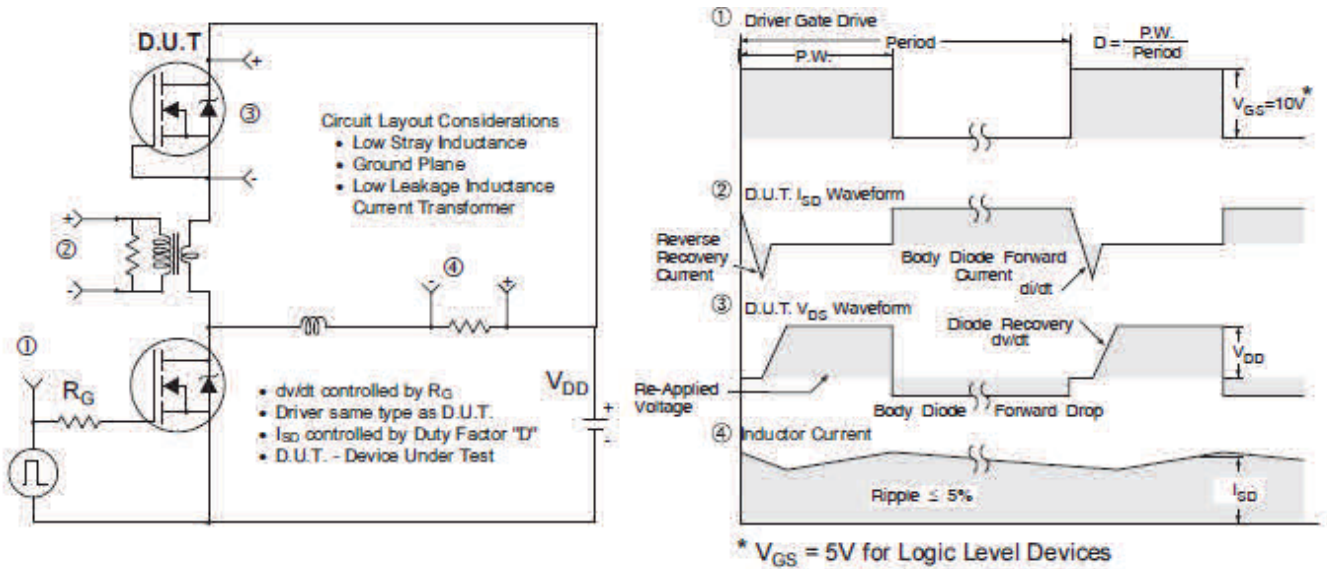
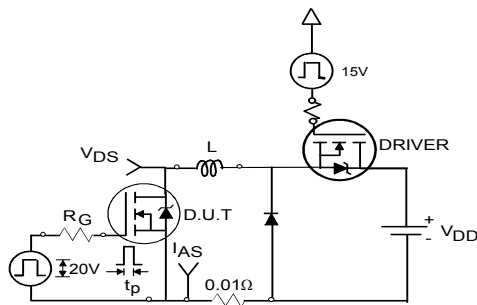
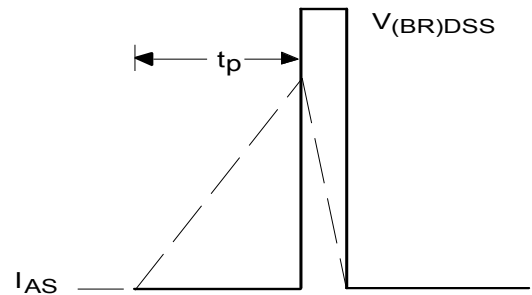
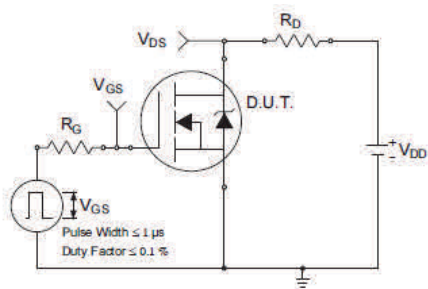
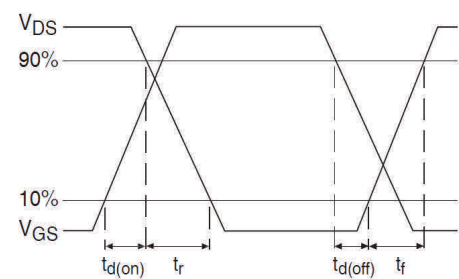
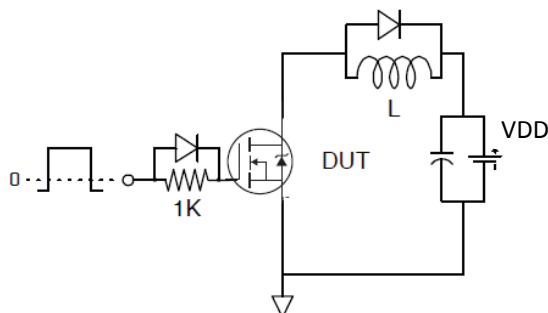
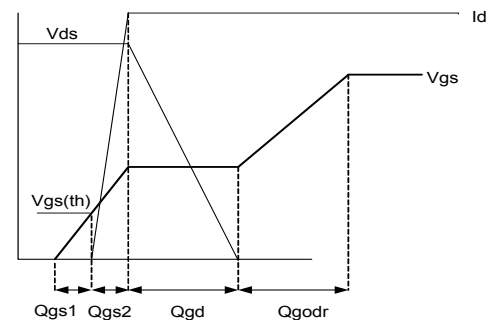

**Fig 3. Typical Output Characteristics**

**Fig 4. Typical Output Characteristics**

**Fig 5. Typical Transfer Characteristics**

**Fig 6. Normalized On-Resistance vs. Temperature**

**Fig 7. Typical Capacitance vs. Drain-to-Source Voltage**

**Fig 8. Typical Gate Charge vs. Gate-to-Source Voltage**


**Fig 9.** Typical Source-Drain Diode Forward Voltage

**Fig 10.** Maximum Safe Operating Area

**Fig 11.** Drain-to-Source Breakdown Voltage

**Fig 12.** Typical  $C_{oss}$  Stored Energy

**Fig 13.** Typical On-Resistance vs. Drain Current

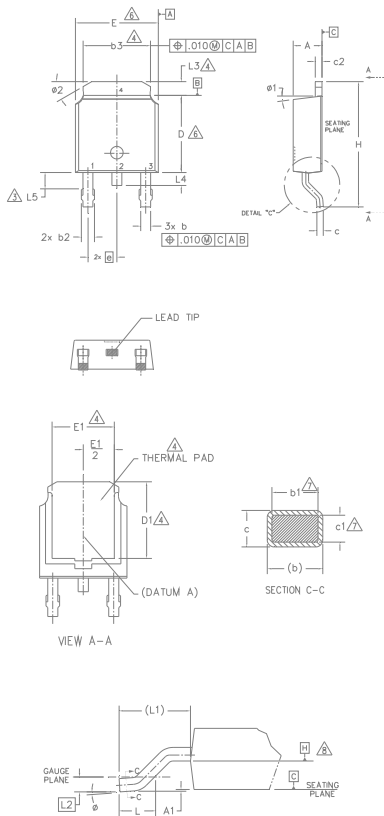

**Fig 14. Maximum Effective Transient Thermal Impedance, Junction-to-Case**

**Fig 15. Avalanche Current vs. Pulse Width**

**Fig 16. Maximum Avalanche Energy vs. Temperature**
**Notes on Repetitive Avalanche Curves , Figures 15, 16:  
(For further info, see AN-1005 at www.irf.com)**

1. Avalanche failures assumption:  
Purely a thermal phenomenon and failure occurs at a temperature far in excess of  $T_{jmax}$ . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as  $T_{jmax}$  is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 23a, 23b.
4.  $P_{D(ave)}$  = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6.  $I_{av}$  = Allowable avalanche current.
7.  $\Delta T$  = Allowable rise in junction temperature, not to exceed  $T_{jmax}$  (assumed as 25°C in Figure 15, 16).  
 $t_{av}$  = Average time in avalanche.  
 $D$  = Duty cycle in avalanche =  $t_{av} \cdot f$   
 $Z_{thJC}(D, t_{av})$  = Transient thermal resistance, see Figures 13)  
 $P_{D(ave)} = 1/2 ( 1.3 \cdot BV \cdot I_{av} ) = \Delta T / Z_{thJC}$   
 $I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$   
 $E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$


**Fig 17.** Threshold Voltage vs. Temperature

**Fig 18.** Typical Recovery Current vs.  $di_F/dt$ 

**Fig 19.** Typical Recovery Current vs.  $di_F/dt$ 

**Fig 20.** Typical Stored Charge vs.  $di_F/dt$ 

**Fig 21.** Typical Stored Charge vs.  $di_F/dt$


**Fig 22. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs**

**Fig 23a. Unclamped Inductive Test Circuit**

**Fig 23b. Unclamped Inductive Waveforms**

**Fig 24a. Switching Time Test Circuit**

**Fig 24b. Switching Time Waveforms**

**Fig 25a. Gate Charge Test Circuit**

**Fig 25b. Gate Charge Waveform**



**D-Pak (TO-252AA) Package Outline (Dimensions are shown in millimeters (inches))**

**NOTES:**

- 1.- DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
- 2.- DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS]
- 3.- LEAD DIMENSION UNCONTROLLED IN L5.
- 4.- DIMENSION D1, E1, L3 & b3 ESTABLISH A MINIMUM MOUNTING SURFACE FOR THERMAL PAD.
- 5.- SECTION C-C DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 AND 0.10 [0.13 AND 0.25] FROM THE LEAD TIP.
- 6.- DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .006 [0.15] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
- 7.- DIMENSION b1 & c1 APPLIED TO BASE METAL ONLY.
- 8.- DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
- 9.- OUTLINE CONFORMS TO JEDEC OUTLINE TO-252AA.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	2.18	2.39	.086	.094	
A1	-	0.13	-	.005	
b	0.64	0.89	.025	.035	
b1	0.64	0.79	.025	.031	7
b2	0.76	1.14	.030	.045	
b3	4.95	5.46	.195	.215	4
c	0.46	0.61	.018	.024	
c1	0.41	0.56	.016	.022	7
c2	0.46	0.89	.018	.035	
D	5.97	6.22	.235	.245	6
D1	5.21	-	.205	-	4
E	6.35	6.73	.250	.265	6
E1	4.32	-	.170	-	4
e	2.29 BSC		.090 BSC		
H	9.40	10.41	.370	.410	
L	1.40	1.78	.055	.070	
L1	2.74 BSC		.108 REF.		
L2	0.51 BSC		.020 BSC		
L3	0.89	1.27	.035	.050	4
L4	-	1.02	-	.040	
L5	1.14	1.52	.045	.060	3
ø	0"	10"	0"	10"	
ø1	0"	15"	0"	15"	
ø2	25"	35"	25"	35"	

**LEAD ASSIGNMENTS**
**HEXFET**

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

**IGBT & CoPAK**

- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER
- 4.- COLLECTOR

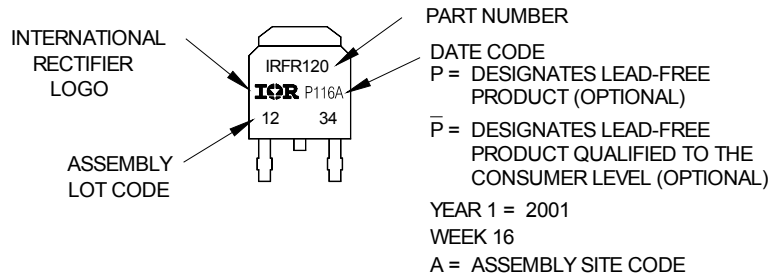
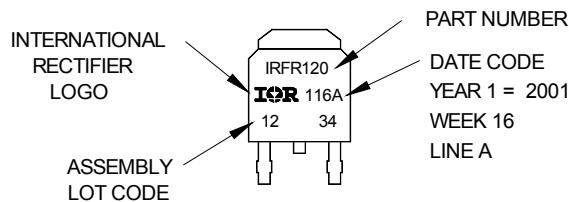
**D-Pak (TO-252AA) Part Marking Information**

EXAMPLE: THIS IS AN IRFR120  
WITH ASSEMBLY  
LOT CODE 1234  
ASSEMBLED ON WW 16, 2001  
IN THE ASSEMBLY LINE "A"

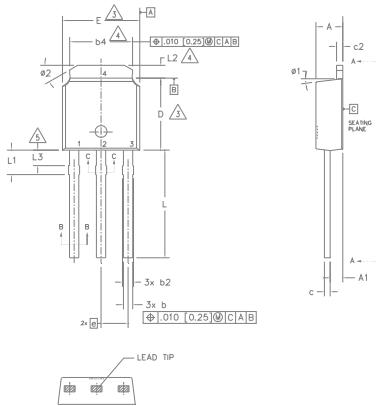
Note: "P" in assembly line position  
indicates "Lead-Free"

"P̄" in assembly line position indicates  
"Lead-Free" qualification to the consumer-level

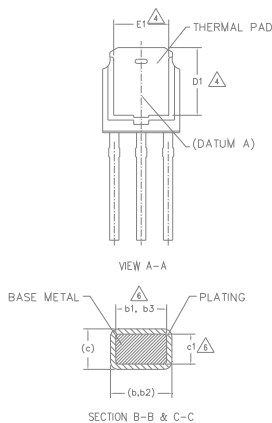
OR



Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

**I-Pak (TO-251AA) Package Outline (Dimensions are shown in millimeters (inches))**


- NOTES:
- 1.- DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
  - 2.- DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS].
  - 3.- DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005 [.013] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
  - 4.- THERMAL PAD CONTOUR OPTION WITHIN DIMENSION b4, L2, E1 & D1.
  - 5.- LEAD DIMENSION UNCONTROLLED IN L3.
  - 6.- DIMENSION b1, b3 & c1 APPLY TO BASE METAL ONLY.
  - 7.- OUTLINE CONFORMS TO JEDEC OUTLINE TO-251AA (Date 06/02).
  - 8.- CONTROLLING DIMENSION : INCHES.



SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	2.18	2.39	.086	.094	
A1	0.89	1.14	.035	.045	
b	0.64	0.89	.025	.035	
b1	0.65	0.79	.025	.031	6
b2	0.76	1.14	.030	.045	
b3	0.76	1.04	.030	.041	6
b4	4.95	5.46	.195	.215	4
c	0.46	0.61	.018	.024	
c1	0.41	0.56	.016	.022	6
c2	0.46	0.89	.018	.035	
D	5.97	6.22	.235	.245	3
D1	5.21	-	.205	-	4
E	6.35	6.73	.250	.265	3
E1	4.32	-	.170	-	4
e	2.29 BSC		.090 BSC		
L	8.89	9.65	.350	.380	
L1	1.91	2.29	.045	.090	
L2	0.89	1.27	.035	.050	4
L3	0.89	1.52	.035	.060	5
phi1	0"	15"	0"	15"	
phi2	25"	35"	25"	35"	

LEAD ASSIGNMENTS

HEXFET

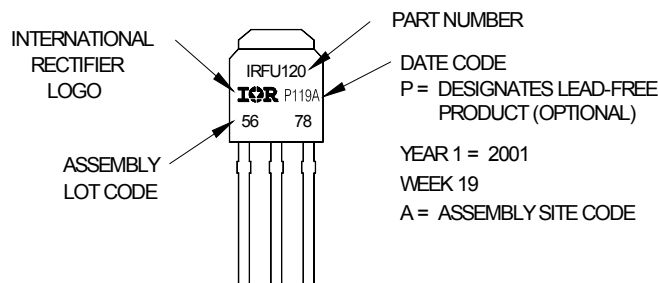
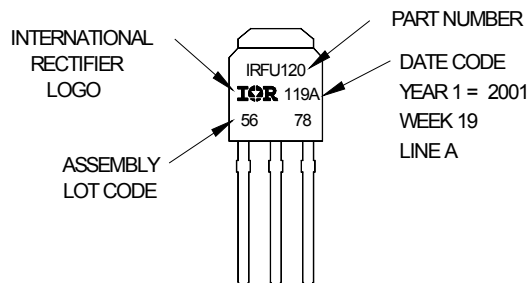
- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

**I-Pak (TO-251AA) Part Marking Information**

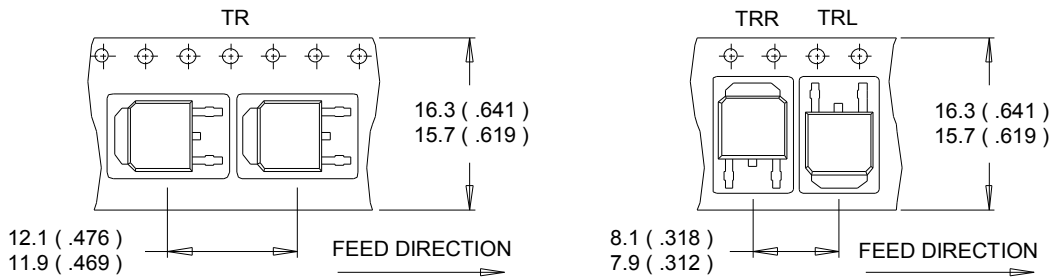
EXAMPLE: THIS IS AN IRFU120  
WITH ASSEMBLY  
LOT CODE 5678  
ASSEMBLED ON WW 19, 2001  
IN THE ASSEMBLY LINE "A"

Note: "P" in assembly line position  
indicates Lead-Free"

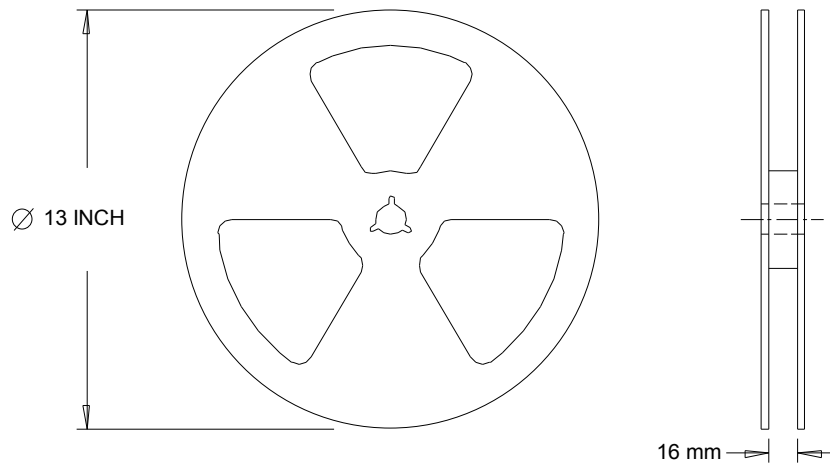
OR



Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

**D-Pak (TO-252AA) Tape & Reel Information (Dimensions are shown in millimeters (inches))**


- NOTES :
1. CONTROLLING DIMENSION : MILLIMETER.
  2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS ( INCHES ).
  3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



- NOTES :
1. OUTLINE CONFORMS TO EIA-481.

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

**Qualification Information<sup>†</sup>**

<b>Qualification Level</b>	Industrial (per JEDEC JESD47F) <sup>††</sup>	
<b>Moisture Sensitivity Level</b>	D-Pak	MSL1
	I-Pak	
<b>RoHS Compliant</b>	Yes	

† Qualification standards can be found at International Rectifier's web site: <http://www.irf.com/product-info/reliability/>

†† Applicable version of JEDEC standard at the time of product release.

**Revision History**

<b>Date</b>	<b>Comment</b>
11/5/2014	<ul style="list-style-type: none"> <li>• Updated <math>E_{AS (L=1mH)} = 242mJ</math> on page 2</li> <li>• Updated note 9 "Limited by <math>T_{Jmax}</math>, starting <math>T_J = 25^{\circ}C</math>, <math>L = 1mH</math>, <math>R_G = 50\Omega</math>, <math>I_{AS} = 22A</math>, <math>V_{GS} = 10V</math>" on page 2</li> </ul>